TTC STANDARDS

JJ-50.20

Digital Transmission System on Optical Local Lines for Leased Line Service of up to 6144 kbit/s

(English Edition)

Version 1

April 22,1999

THE TELECOMMUNICATION TECHNOLOGY COMMITTEE

Introduction

This document is an English translated document of JJ-50.20 version 1 Japanese Edition. JJ-50.20 provides the TTC original Standard formulated and put into effect by the Technical Assembly. It contains unabbreviated version of ‘JJ-‘ Standard, which has not been defined as international standard.

In case of dispute, the original to be referred is the Japanese edition of the text.

We trust that greater understanding of TTC Standards by a wider range of users will further contribute to the development of telecommunications.

April 22, 1999

JJ－50.20 Digital Transmission System on Optical Local Lines for Leased Line Service of up to 6144 kbit／s

1. Relation to international recommendations

This standard specifies the transmission interface of digital transmission system on optical local lines for digital leased line service of up to 6144 kbit/s in Japan.

2. History of revision

Version	History of Revision Dates	Remarks
Version 1	1999.4.22	Established

3. Others

(1) Referred recommendations and regulations

TTC standards : JT-G703, JT-I431a

ITU-T recommendations : G.651, G.652, G.704

JIS : C5973

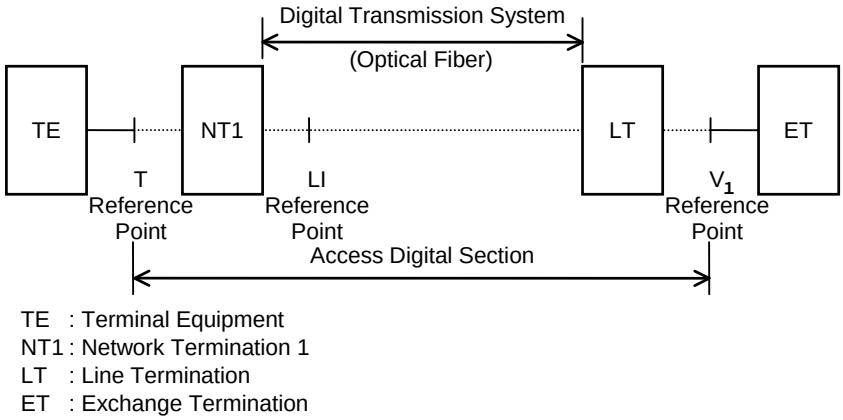
Contents

1. Relation to International recomendations

This standard describes the characteristics and parameters of optical interface (LI reference point) at network side of the NT1 for digital leased line service between 64kbit/s and 6144kbit/s.

2. Reference Configuration

The Figure 2-1/JJ-50.20 describes the scope of access digital section in reference to digital transmission system.



TE : Terminal Equipment
NT1 : Network Termination 1
LT : Line Termination
ET : Exchange Termination

FIGURE 2-1/JJ-50.20 Scope of Access Digital Section and Transmission System

3. Interface Description

The interface described in this standard consist of the following requirements.

(1) Physical Requirements

Figure, dimensional specification of connector for the connection of optical fiber cable and NT1.

(2) Optical Requirements

Specification of optical signal at LI reference point for the connection of optical fiber cable and NT1.

(3) Logical Requirements

Methods and operating requirements for signal transmission between optical fiber cable and NT1.

Operation and maintenance issues are discussed from chapter 4.

3.1 Physical Requirements

(1) Optical Connector

Two (input and output) F04 single optical fiber connectors (JIS C5973) are used for optical transmission of NT1.

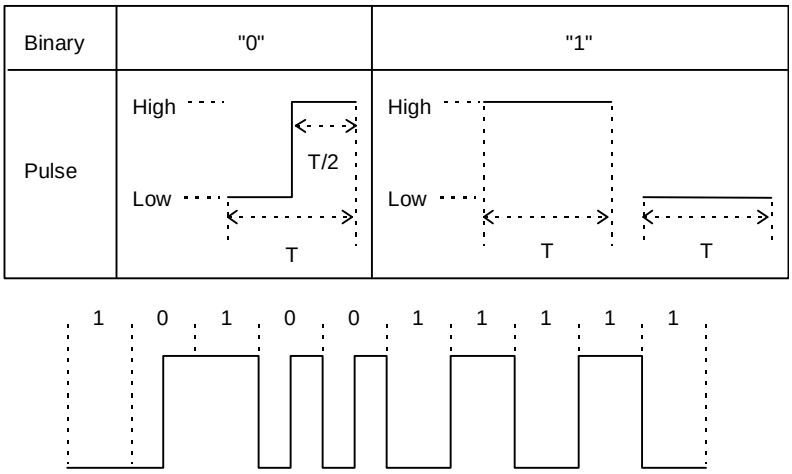
(2) Optical Fiber Cable

NT1 is required to be compatible with both multimode graded index (GI) optical fiber cable that conform with ITU-T Recommendation G.651 (or IEC standard A1a) and single-mode (SM) optical fiber cable that conform with ITU-T Recommendation G.652 (or IEC standard B1.1a).

3.2 Optical Requirements

(1) Transmission Code

CMI code is used. CMI (Coded Mark Inversion) is a 2-level non-return-to-zero code in which binary "0" corresponds to levels "L" and "H" consecutively for each half unit time interval (T/2) , and binary "1" corresponds to "H" and "L" alternately for one unit time interval (T) as shown in Figure 3-1/JJ-50.20. (The level "L" represents "Low", "H" represents "High", respectively.)



(Note 1) Positive logic shall be used. So that optical power should be turned on at CMI code "H" and off at CMI code "L" respectively.

(Note 2) $T = 1 / 6.312 \times 10^{-6}$ [s]

FIGURE 3-1/JJ-50.20 Explanation of CMI Code

(2) Specification of the optical output level

The specification of the optical output level for signals sent from NT1 to LT is shown in the Table 3-1/JJ-50.20.

TABLE 3-1/JJ-50.20 Specification of the optical output level

Items	Specification
Optical Transmitted Power	-19.0 ～ -10.0dBm
Transmission Wavelength (Typ.Value)	1.270 ～ 1.335μm
Spectral Characteristics	≦10nm
Extinction Ratio (EX)	≧11dB
Optical Pulse Width	79.2±15.8ns

An example of the optical waveform is shown in Figure 3-2/JJ-50.20.

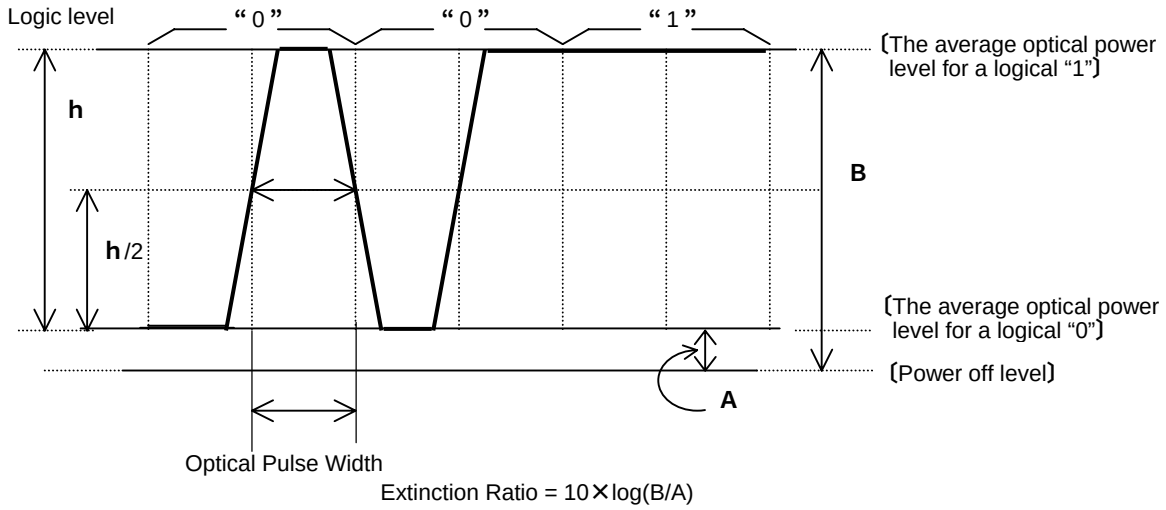


FIGURE 3-2/JJ-50.20 Example of optical waveform

(3) Duty Ratio

It is 100 ± 20% of the optical pulse width shown in Figure 3-2/JJ-50.20. But, it is defined at 50% of the pulse amplitude.

(4) Jitter

It is ± 10% of the optical pulse width shown in the Figure 3-2/JJ-50.20.

(5) Specification of optical input level

a)Specification of optical input level

The average optical input level which is received NT1 is greater than –36 .8dBm, and less than –11.0dBm.

b) Performance required for NT1.

① Error performance

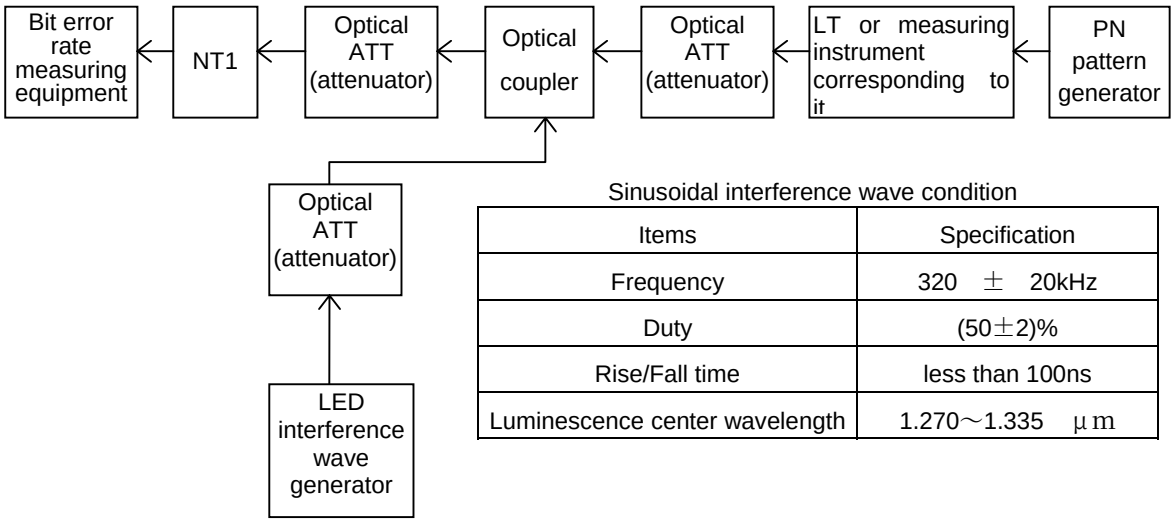
For the circuit shown in Figure 3-3/JJ-50.20, when an optical interference waveform of S/X=8dB is added to an optical signal whose average optical input level at input terminal LI of NT1 is –36.8dBm, the bit error rate must be less than 10^{-6}.

② Characteristic of maximum received power.

For the circuit shown in Figure 3-3/JJ-50.20, when no optical interference waveform is added to an optical signal whose average optical input level at input terminal LI of NT1 is –11.0dBm, the bit error rate must be less than 10^{-6}.

③ Optical level variation tolerance

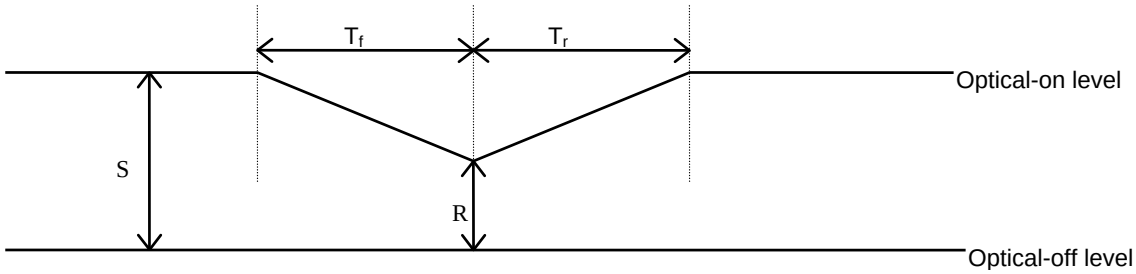
For the circuit shown in Figure 3-3/JJ-50.20, when the average optical input level at input terminal LI of NT1 is set to –32.0 dBm, the bit error rate for the optical level variation waveform shown in Figure 3-4/JJ-50.20 must be less than 10^{-8}.



Sinusoidal interference wave condition

Items	Specification
Frequency	320 ± 20kHz
Duty	(50±2)%
Rise/Fall time	less than 100ns
Luminescence center wavelength	1.270～1.335 μm

FIGURE.3-3 / JJ-50.20 Bit error rate measuring circuit



- $10 \times \log(S/R) = 3.5 \pm 0.5$dB
- T_f, $T_r = 200 \pm 10$ μs
- This waveform repeats itself with the period of 10±1ms.

FIGURE 3-4 / JJ-50.20 Optical level variation waveform

3.3 Logical condition

(1) Frame structure transferred on the subscriber's line

a) Transmission rate

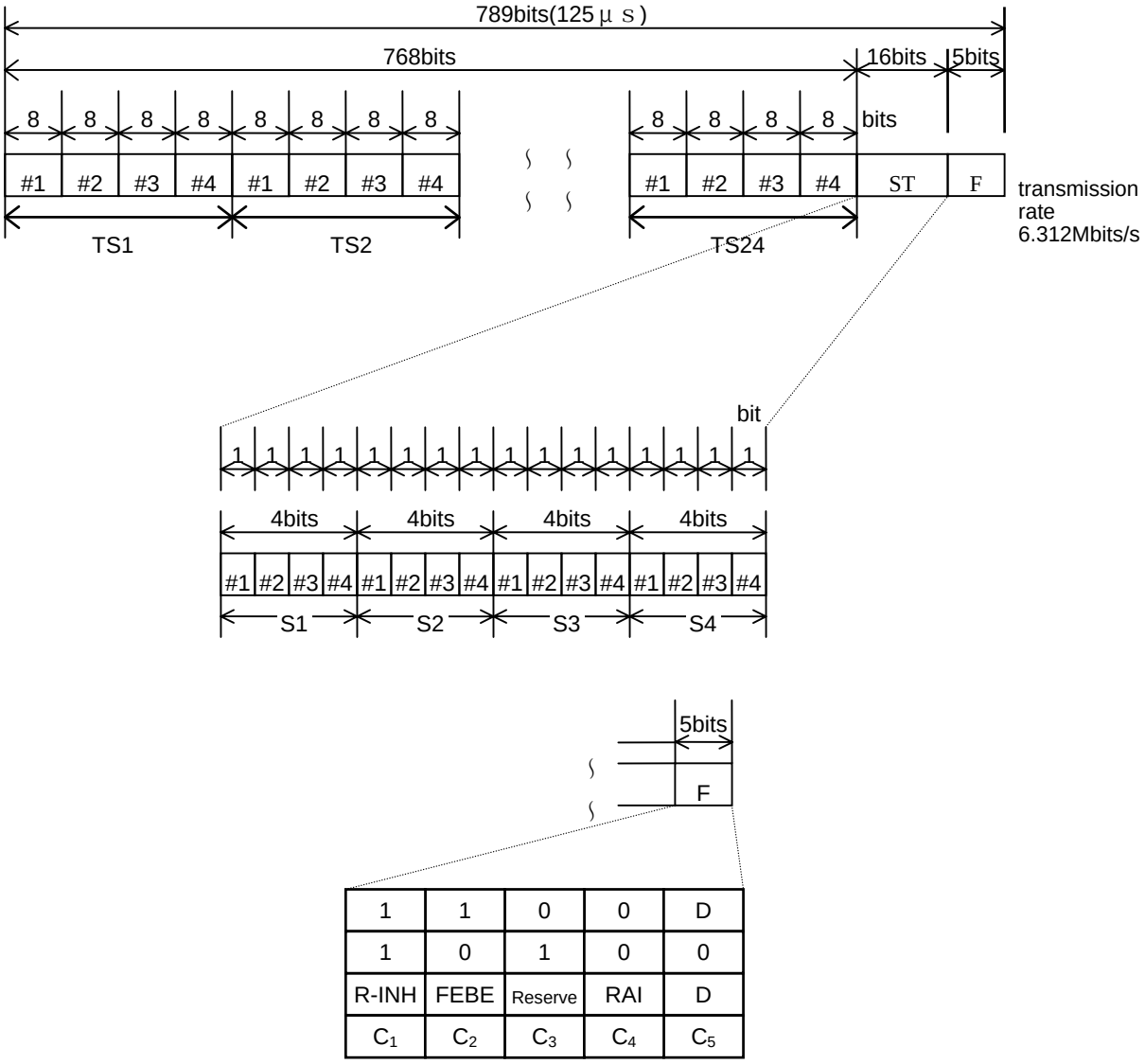
Transmission rate is defined to be 6.312Mbits/s.

b) Frame structure

6.312Mbits/s interface frame is constructed by a multiframe that is composed of four 1.5Mbits/s logical path frames and administration/management bits (Fbits).

6.312Mbits/s interface frame is shown in Figure 3-5 / JJ-50.20, 1.5Mbits/s logical path frame is shown in Figure 3-6 / JJ-50.20.

Furthermore, TS1～TS24(768bits) are used as information channels ,and each ST(16bits) and F(5bits) bits are used as operation, administration and management bits in the 6.312Mbits/s interface frame.



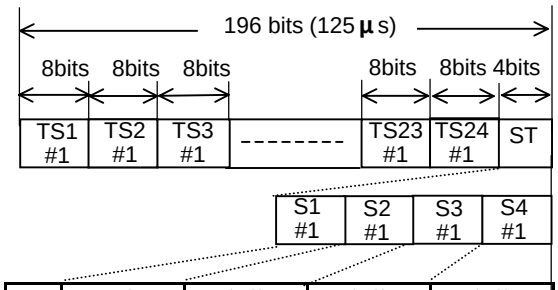
1	1	0	0	D
1	0	1	0	0
R-INH	FEBE	Reserve	RAI	D
C_1	C_2	C_3	C_4	C_5

Note 1: #1～#4 in this figure represent the 1.5Mbits/s logical path (24TSs+4bits in ST) number, and each path must be structured as shown in Figure 3-6 / JJ-50.20.

Note 2: F Bit Definition

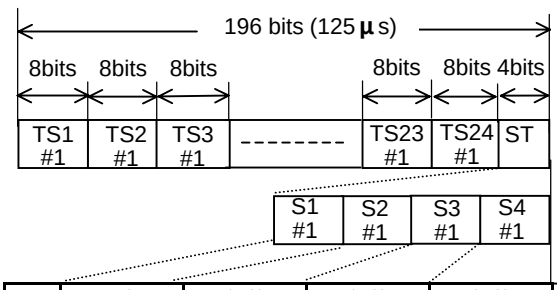
Bits	Details
D	Data Link (fixed “0”)
RAI	Normal operation: “0” , Alarm “1”
FEBE	Normal operation: “0” , Alarm “1”
R-INH	Normal operation: “0” , NT1 Powered off: “1”refer to Chapter 5
C	Bit error monitor (CRC-5〈 generating polynomial: $X^5+X^4+X^2+1$〉)
Reserved	fixed “1”

FIGURE 3-5 / JJ-50.20 6.312Mbits/s interface frame structure



1	FS	(FS)	(FS)	(FS)
2	*	*	*	*
⟆	⟆	⟆	⟆	⟆
7	*	*	*	*
8	1.5MFERF	Kx	*	*
9	FS	(FS)	(FS)	(FS)
10	*	*	*	*
⟆	⟆	⟆	⟆	⟆
16	*	*	*	*
17	FS	(FS)	(FS)	(FS)
18	*	*	*	*
⟆	⟆	⟆	⟆	⟆
23	*	*	*	*
24	“ 1 ”	“ 1 ”	“ 1 ”	“ 1 ”
25	FS	(FS)	(FS)	(FS)
26	*	*	*	*
⟆	⟆	⟆	⟆	⟆
31	*	*	*	*
32	“ 1 ”	“ 1 ”	“ 1 ”	“ 1 ”
33	FS	(FS)	(FS)	(FS)
34	LP2	*	*	*
35	*	*	*	*
⟆	⟆	⟆	⟆	⟆
39	*	*	*	*
40	“ 1 ”	“ 1 ”	“ 1 ”	“ 1 ”
41	FS	(FS)	(FS)	(FS)
42	*	*	*	*
⟆	⟆	⟆	⟆	⟆
47	*	*	*	*
48	“ 1 ”	“ 1 ”	“ 1 ”	“ 1 ”
49	FS	(FS)	(FS)	(FS)
50	*	*	*	*
⟆	⟆	⟆	⟆	⟆
55	*	*	*	*
56	“ 1 ”	“ 1 ”	“ 1 ”	“ 1 ”
57	FS	(FS)	(FS)	(FS)
58	*	*	*	*
⟆	⟆	⟆	⟆	⟆
63	*	*	*	*
64	“ 1 ”	“ 1 ”	“ 1 ”	“ 1 ”

LT → NT1



1	FS	(FS)	(FS)	(FS)
2	“ 0 ”	“ 0 ”	“ 0 ”	“ 0 ”
⟆	⟆	⟆	⟆	⟆
7	“ 0 ”	“ 0 ”	“ 0 ”	“ 0 ”
8	1.5MFERF	Kx	“ 0 ”	“ 0 ”
9	FS	(FS)	(FS)	(FS)
10	“ 0 ”	“ 0 ”	“ 0 ”	“ 0 ”
⟆	⟆	⟆	⟆	⟆
16	“ 0 ”	“ 0 ”	“ 0 ”	“ 0 ”
17	FS	(FS)	(FS)	(FS)
18	“ 0 ”	“ 0 ”	“ 0 ”	“ 0 ”
⟆	⟆	⟆	⟆	⟆
23	“ 0 ”	“ 0 ”	“ 0 ”	“ 0 ”
24	“ 1 ”	“ 1 ”	“ 1 ”	“ 1 ”
25	FS	(FS)	(FS)	(FS)
26	“ 0 ”	“ 0 ”	“ 0 ”	“ 0 ”
⟆	⟆	⟆	⟆	⟆
31	“ 0 ”	“ 0 ”	“ 0 ”	“ 0 ”
32	“ 1 ”	“ 1 ”	“ 1 ”	“ 1 ”
33	FS	(FS)	(FS)	(FS)
34	“ 0 ”	“ 0 ”	“ 0 ”	“ 0 ”
35	“ 0 ”	“ 0 ”	“ 0 ”	“ 0 ”
⟆	⟆	⟆	⟆	⟆
39	“ 0 ”	“ 0 ”	“ 0 ”	“ 0 ”
40	“ 1 ”	“ 1 ”	“ 1 ”	“ 1 ”
41	FS	(FS)	(FS)	(FS)
42	“ 0 ”	“ 0 ”	“ 0 ”	“ 0 ”
⟆	⟆	⟆	⟆	⟆
47	“ 0 ”	“ 0 ”	“ 0 ”	“ 0 ”
48	“ 1 ”	“ 1 ”	“ 1 ”	“ 1 ”
49	FS	(FS)	(FS)	(FS)
50	“ 0 ”	“ 0 ”	“ 0 ”	“ 0 ”
⟆	⟆	⟆	⟆	⟆
55	“ 0 ”	“ 0 ”	“ 0 ”	“ 0 ”
56	“ 1 ”	“ 1 ”	“ 1 ”	“ 1 ”
57	FS	(FS)	(FS)	(FS)
58	“ 0 ”	“ 0 ”	“ 0 ”	“ 0 ”
⟆	⟆	⟆	⟆	⟆
63	“ 0 ”	“ 0 ”	“ 0 ”	“ 0 ”
64	“ 1 ”	“ 1 ”	“ 1 ”	“ 1 ”

8ms

NT1 → LT

(Note) Bit Definition

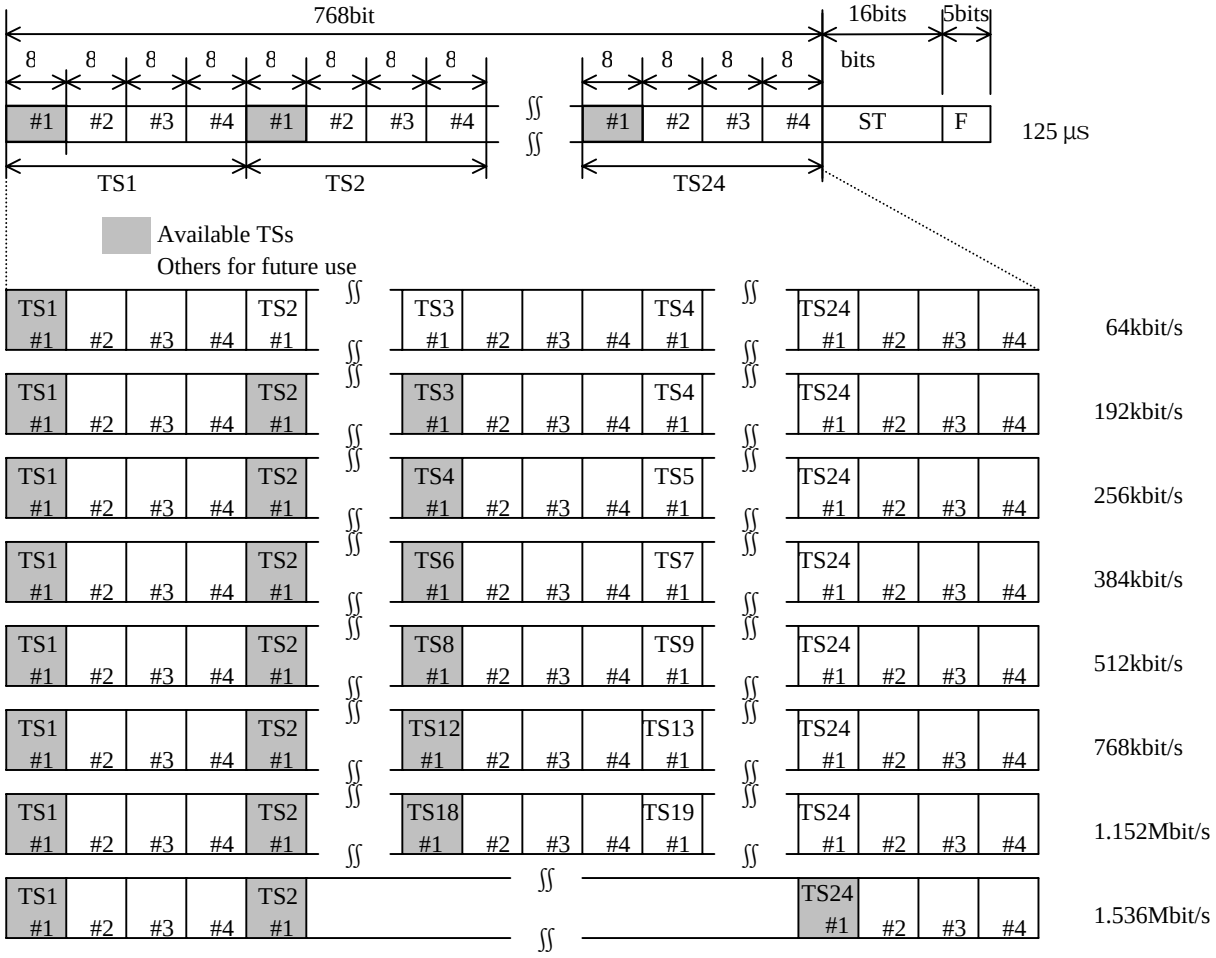
Symbol	Details
Kx	Switching control bit of subscriber line (refer to Chapter6)
1.5M FERF	"1":When 1.5M AIS or 1.5M LOF is detected, "0":Normal Operation
LP2	"1": When loopback2 test is executed, "0":Other
*	Undefined

FIGURE 3-6/JJ-50.20 1.5M bit/s logical path frame structure

c） TS allocation method

Two methods are used for allocating TSs to convey user data.

Pattern A which is used for basic services under 1.5Mbit/s is shown in Figure 3-7/JJ-50.20, and pattern B which contains the basic services over 1.5Mbit/s is shown in Figure 3-8/JJ-50.20. The allocation methods of TSs are determined by the rate of the basic services.

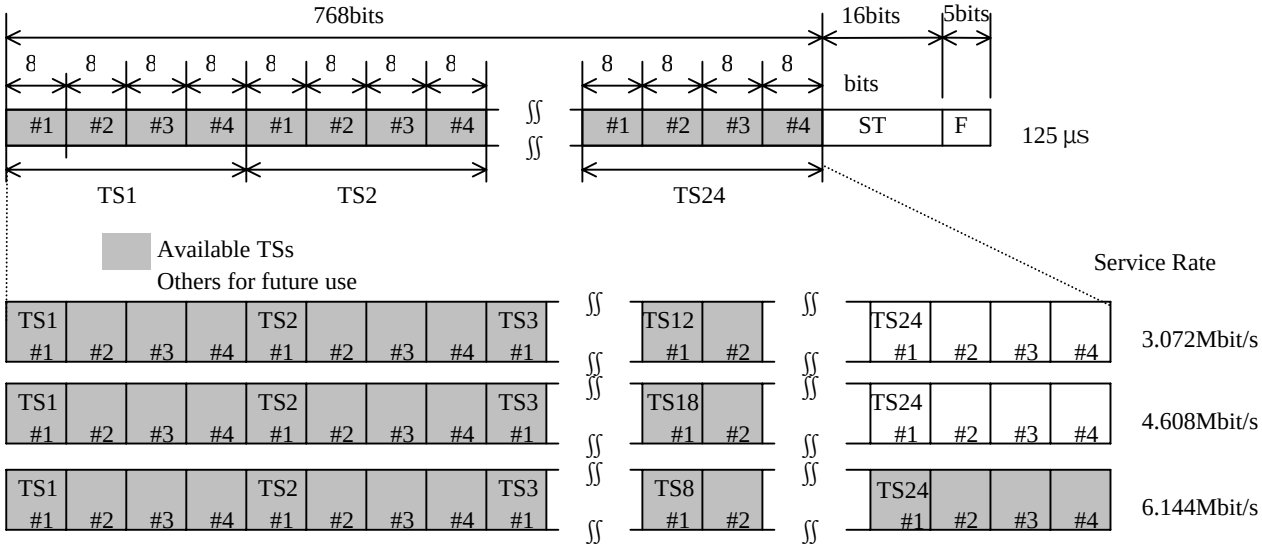


（Order of Time Slot Allocation：ＴＳ１　＃１　→　ＴＳ２　＃１　→　ＴＳ３　＃１　．．．　）

Rate of basic service	Time slots used	Rate of basic service	Time slots used
64kbit/s	TS1#1	512kbit/s	TS1#1～TS8#1
192kbit/s	TS1#1～TS3#1	768kbit/s	TS1#1～TS12#1
256kbit/s	TS1#1～TS4#1	1.152Mbit/s	TS1#1～TS18#1
384kbit/s	TS1#1～TS6#1	1.536Mbit/s	TS1#1～TS24#1

FIGURE 3-7/JJ-50.20　Example of time slots allocation over optical local lines (Pattern A)

（Shows the TSs allocation for the rates of basic services.）



（Order of the Time Slots Allocation：ＴＳ１　＃１　→　ＴＳ１　＃２　→　ＴＳ１　＃３　．．．　）

Rate of basic service	Time slots used
3.072Mbit/s	TS1#1～TS12#4
4.608Mbit/s	TS1#1～TS18#4
6.144Mbit/s	TS1#1～TS24#4

FIGURE 3-8/JJ-50.20　Example of Time Slots allocation over optical local lines (Pattern B)

（It is shown the examples of the TSs allocation for the rates of basic services. ）

（２）Frame Synchronization

The 6.312Mbit/s interface frame synchronization and the 1.5Mbit/s logical frame synchronization are to be performed independently.　The positions of the first frame for both frames is prohibited to be the same.

ａ）　6.312Mbit/s Interface Frame

The code for multiframe word is “110010100”.

The transmission system is considered to enter the loss of multiframe alignment state if the multiframe word has not been identified for seven consecutive frames while in the multiframe alignment state. The transmission system is considered to enter the multiframe alignment state if the multiframe word has been identified for three consecutive frames while in the loss of multiframe alignment state.

Detection of more than one error bit in the multiframe word “110010100” is counted as one frame not identified, while detection of zero error bit in the multiframe word “110010100” is counted as one frame identified.

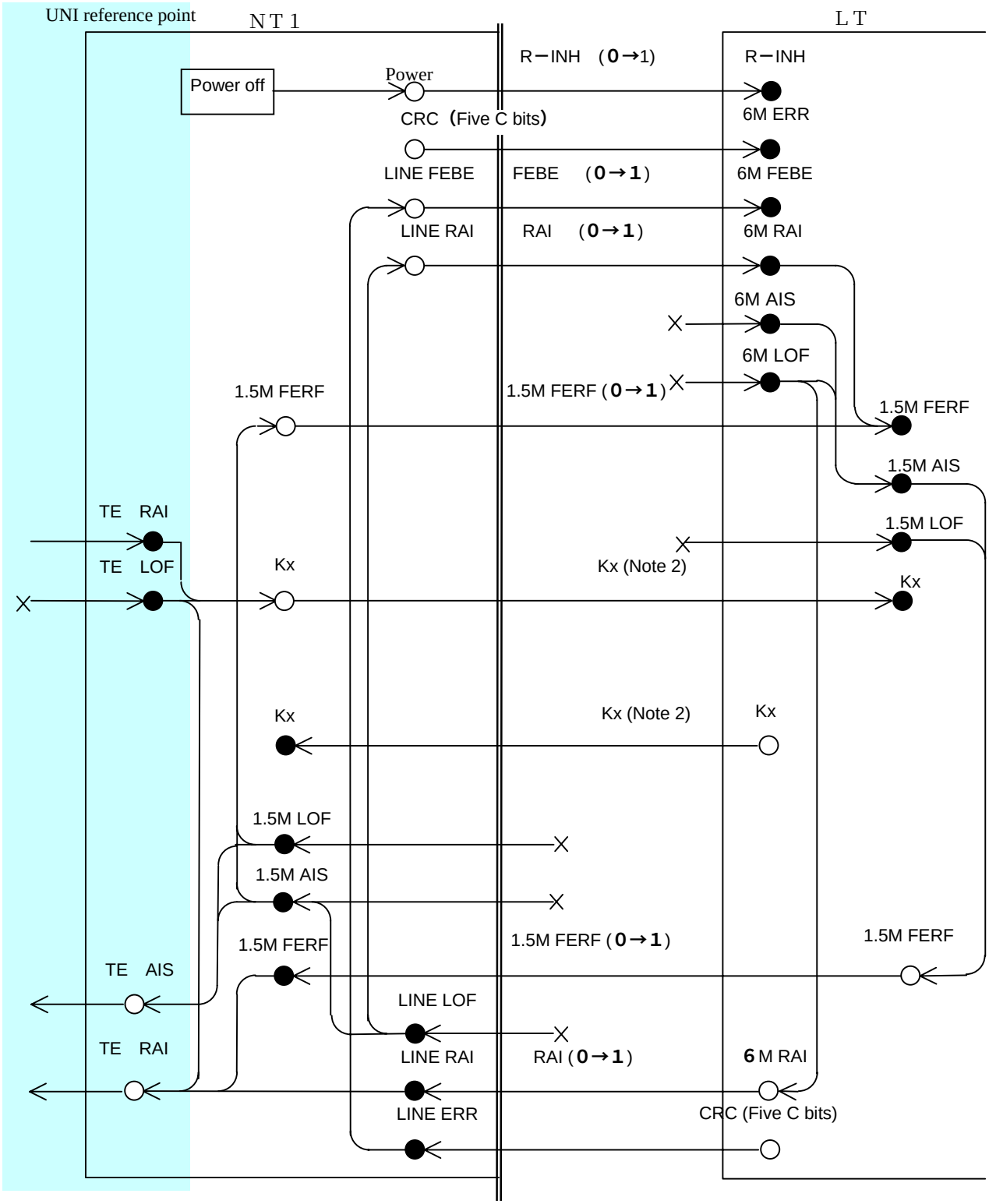
ｂ）　1.5Mbit/s Logical Path Frame

The code for the frame word of FS is　“11010110 11000001 100110110 10011100 11110110 10000101”.

The transmission system is considered to enter the loss of frame alignment state if the frame word in S1, which is described in Figure 3-6/JJ50.20, has not been identified for four consecutive frames while in the frame alignment state. The transmission system is considered to enter the frame alignment state if the frame word in S1 has been identified for two consecutive frames while in the loss of frame alignment state.

4. Transmission of Operation and Maintenance Information

Figure 4-1/JJ-50.20 indicates the maintenance information transmission diagram. Main operation and maintenance functions are described below.



(Note1) □ region is shown for the case where the User-Network Interface of TE-NT1 is based on TTC standard JT-I431a, JT-G703-a.

●：Detection point
○：Originating point
×：Defect and failure detection

(Note2) Refer to chapter 6 for Kx.

(Note3) AIS:Alarm Indication Signal

FIGURE 4-1/JJ-50.20 Alarm Transmission diagram

4.1 The transfer of the main signal as all '1'

When a relay section or a terminal section breaks down (break, a synchronous disconnection) make all the information channels in the trouble direction "1".

(Only all the parts which cope with a trouble circuit are made "1" in the case of the multiplex access.)

4.2 Monitoring of bit error

(1) CRC(Cyclic Redundancy Check) method

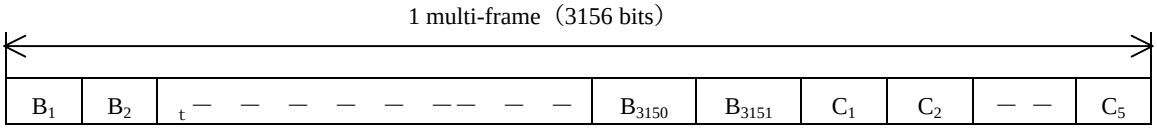
Detection of bit error is performed by the CRC method. CRC method is based on the TTC standard JT-G704.

The message block (CMB) of CRC is a 3151 bit sequence which begins from the 1st bit of the 1st frame, and ends at the 784th bit of the 4th frame.

As shown in Figure 4-2/JJ-50.20, message block check bits (CRC -5 bits) C1, C2, C3, C4, C5 are placed at the last 5 bits of the multiframe. Their values are the remainder (modulo2) obtained when the Nth CMB is multiplied by X^5 and then divided by the generating polynomial $X^5+X^4+X^2+1$.

The first check bit (C1) is the MSB of the remainder, and the last check bit (C5) is the LSB. Each multi-frame contains CRC -5 bits obtained from its CMB.

At the receiving end, if there are no transmission errors, the remainder of 3156 bit sequence (3151 CMB bits and 5 CRC bits) divided by the generating polynomial should result in the value "00000".



* " $C_1X^4+C_2X^3+C_3X^2+C_4X+C_5$ " is the remainder (modulo2) when

" $X^5 (B_1X^{3150}+B_2X^{3149}+\cdots\cdots+B_{3150}X+B_{3151})$ " is divided by

"$X^5+X^4+X^2+1$"

FIGURE 4-2/JJ-50.20 CRC bit method

(2) Transmission of bit error detection information

When bit errors (CRC error) are detected in the input signal, one bit of bit error detection information must be transmitted to LT1 for each bit error detected

4.3 Failure in the downstream direction

When LINE LOF is detected, NT1 must transmit upstream RAI bit as "1" to LT.

When 1.5M LOF or 1.5M AIS is detected, NT1 must transmit upstream 1.5M FERF as "1" to LT.

4.4 Failure in the upstream direction

During failure in the upstream direction, LT sends RAI bit as "1" and 1.5M FERF as "1" to NT1.

4.5 Detection and clear conditions of transmission failure

Detection and clear conditions of various transmission failures are shown in Table 4-1/JJ-50.20.

TABLE 4-1/JJ-50.20　Detection and clear conditions of Transmission failures

Type	Detection condition	Clear condition
Loss of Frame (LINE LOF or 6M LOF)	Frame synchronization pattern undetected for 7 consecutive frames	Frame synchronization pattern detected for 3 consecutive frames
ERR	Error rate of the input pulse, sequence $\geqq 10^{-4}$	The mistake rate of the input pulse line, less than 10^{-6}
Loss of Frame (1.5M LOF)	The frame synchronous pattern inconsistency of the Fs bit in S1,four times continuous detection	The frame synchronous pattern agreement of the Fs bit in S1, two times continuous detection
1.5M AIS	168 consecutive detection of “1”s in the S1 bit sequence	Detection of 5 or more “0”s in a 168 bit sequence of S1

4.6　Detection and clear conditions of operation and maintenance information

Detection and clear conditions of operation and maintenance information are shown in Table 4-2/JJ-50.20.

TABLE 4-2/JJ-50.20　Detection and clear conditions of operation and maintenance information

Type	Detection condition	Clear condition
RAI	Detection of 8 consecutive “1”s	Detection of 3 consecutive “0”s
FEBE	No protection (Instant Detection)	(Instant detection) without protection
R-INH	Detection of 8 consecutive “1”s	Detection of 8 consecutive “0”s for 1～2 seconds
1.5M FERF	Detection of 5 consecutive “1”s	Detection of 5 consecutive “0”s
LP2	Detection of 5 consecutive “1”s	Detection of 5 consecutive “10”s

5. Power supply Off information of NT1 (R-INH bit)

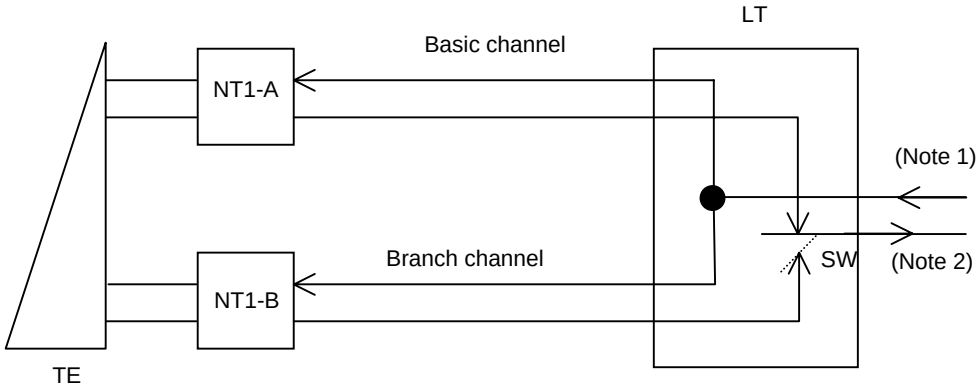
When the power switch and the main power supply is on thethe R-INH bit as " 0", must be sent to the LT .

Also, the R-INH bit must be sent as “0” to the LT when the main power supply as already on, and the power switch is switched “on” from the “off” state, or when the power switch is already on, and the main power supply is turned on. With this procedure, the LT returns to its normal monitoring state.

The R-INH bit must be sent as “1” to the LT for over 16 times, and then go into signal off state when the main power source is already on, and the power switch supply is turned off.

6. Switching control of terminal section by Kx bit

Kx bit is used in order to switch terminal section automatically when a failure is detected between NT1and TE. The structure of the channel is described in Figure 6-1/JJ-50.20.



(Note 1) The communication from LT to NT1 is always broadcast type communication.

(Note 2) The communication from NT1 to LT switches automatically within the LT when basic channel fails.

FIGURE 6-1/JJ-50.20 Switching control of terminal section

6.1 Condition of detecting Kx bit

Condition of detecting Kx bit is described in Figure 6-2/JJ-50.20

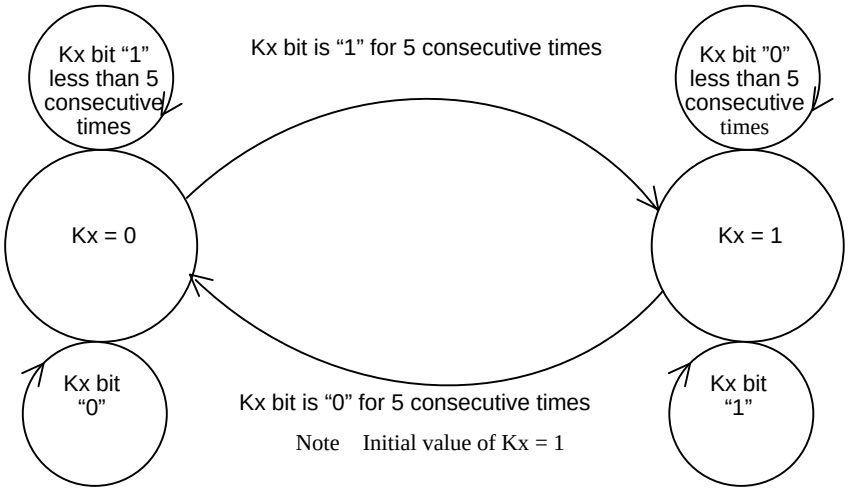


FIGURE 6-2/JJ-50.20 State transition diagram of Kx

6.2 The switching procedure by Kx bit

(1) Kx bit from LT to NT1

The Kx bit of operating channel is "1", the Kx bit of standby channel is "0". For example, for Figure 6-1/JJ-50.20. when NT1-A is the working side (Kx bit of NT1-A is "1", Kx bit of NT1-B is "0") and if a failure is detected in NT1-A, NT1-B side should switch to the working side, and the Kx bit of NT1-A should change to "0", and the Kx bit of NT1-B should change to "1".

(2) Kx bit from NT1 to LT

In the normal state (when the channel is protected by automatic switching), the Kx bits of both working side and standby side are set to "1".

The switching procedure of Kx bit from NT1 to LT in Figure 6-1/JJ-50.20 is shown in Table 6-1/JJ-50.20.

TABLE 6-1/JJ-50.20　Switching Control by Kx bit from NT1 to LT

NT1-A / NT1-B		Working Side		Standby Side	
		Kx = “0”	Kx = “1”	Kx = “0”	Kx = “1”
Working Side	Kx = “0”			No change in state	Switch to NT1-A
	Kx = “1”			No change in state	No change in state
Standby Side	Kx = “0”	No change in state	No change in state		
	Kx = “1”	Switch to NT1-B	No change in state		

7. Loopback function at NT1

For user’s convenience and efficient maintenance during line failure, NT1 must have the following loopback function.

Loopback Test	Description	Control Bit
Loopback 2	Full loopback	LP2 bit

The loopback 2 function is embedded closest to the TE side within NT1.　This allows the determination of whether the malfunction is occurring on the TE side or the NT1 and line side.

7.1 Loopback Condition

The loopback 2 condition and operation are described in Table 7-1/JJ-50.20.

TABLE 7-1/JJ-50.20 Loopback Condition and Operation

Condition		Loopback Operation
Loopback condition	When five or more consecutive “1” s are detected in the LP2 bit of LI as shown in Fig. 3-6/JJ-50.20.	The input signal from LT to NT1 is output from NT1 to LT.
Clear condition	When five or more consecutive “0” s are detected in the LP2 bit of LI as shown in Fig. 3-6/JJ-50.20.	The loopback operation is cleared and returns to normal operation.

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