# TTC STANDARDS

# JJ-50.30

# Physical Layer Specifications of 155520kbit/s Optical

Subscriber Line

Version 1

Nov 25 1999

THE TELECOMMUNICATION TECHNOLOGY COMMITTEE



# Introduction

This document provides the TTC original Standards formulated and put into effect by the Technical Assembly. It contains unabbreviated version of 'JJ-' Standards, which have not been defined as international standards.

In case of dispute, the original to be referred is the Japanese version of the text.

We trust that greater understanding of TTC Standards by a wider range of users will further contribute to the development of telecommunications.

# JJ-50.30 Physical Layer Specifications of 155520kbit/s Optical Subscriber Line

#### 1. Relations with international standards

JJ-50.30 standard describes the physical layer specifications at the line interface (LI) of 155520kbit/s optical subscriber line that provides services such as domestic ATM leased line.

# 2. History of revised versions

Version	Date	Outline		
1	Nov. 25, 1999	Established		

# 3. Others

(1) References

TTC standards: JT-G707 and JT-G957

ITU-T recommendation: G.652

JIS: C5973 and C6835

IEC: 793-2

#### Contents

1. Introduction	1
2. Reference configuration	1
3. Interface conditions	1
3.1 Bit rate	1
3.2 Connector	1
3.3 Transmission medium	1
3.4 Optical conditions	1
3.5 Logical conditions	2
3.5.1 Frame structure	2
3.5.2 Overhead	3
4. Transportation of maintenance and operation information	5
4.1 Alarm transportation diagram	5
4.2 Alarm detection and generation conditions	6
4.3 Power loss information bit of NT1 (R-INH)	7
4.4 Loop information bit (LOOP2)	8

### 1. Introduction

JJ-50.30 standard describes the physical layer specifications at the line interface (LI) of 155520kbit/s optical subscriber line that provides services such as domestic ATM leased line.

#### 2. Reference configuration

Figure 2-1/JJ-50.30 shows the reference configuration. An interface point LI is adjacent to the NT1 on its network side.



- -

Figure 2-1/JJ-50.30 Reference configuration

#### **3. Interface conditions**

#### 3.1 Bit rate

The bit rate at the line interface is 155520kbit/s.

The NT1 transmits signals synchronously with the timing received from the network. In the absence of a valid clock derived from the network, the accuracy of free run frequency is 155520kHz  $\pm 20$ ppm.

#### **3.2 Connector**

An F04 type single optical fiber connector (JIS C 5973) is used at the line interface for transmitting and receiving each.

#### 3.3 Transmission medium

Two optical fibers are used as transmission medium at the line interface. The optical fiber is SM type and complies with ITU-T recommendation G.652 (corresponding to IEC 793-2B1.1a or JIS C 6835 SSMA-10/125).

#### **3.4 Optical conditions**

The optical conditions at the line interface comply with TTC standard JT-G957 L-1.1.

The line coding is scrambled 2-level-NRZ and the convention used for optical logic level is positive (emission of light for a binary '1' and no emission of light for a binary '0').

#### 3.5 Logical conditions

#### 3.5.1 Frame structure

The frame applied to the line interface is STM-1 and the path mapped into STM-1 is only VC-4. The frame structure complies with TTC standard JT-G707. Figure 3-1/JJ-50.30 shows the frame structure.



Figure 3-1/JJ-50.30 Frame structure

#### 3.5.2 Overhead

Figure 3-2/JJ-50.30 shows the mappings of the SOH bytes of STM-1, the POH bytes of VC-4 and the AU-4 pointer.

		1	2	3	4	5	6	7	8	9	byte		
	1	A1	A1	A1	A2	A2	A2	C1 (J0)	+	+		1	J1
STM-1 RSOH	2	B1	-	-	E1	-	-	F1	-	-		2	В3
	3	D1	-	-	D2	-	-	D3	-	-		3	C2
AU-4 POINTER	4	H1	Y	Y	H2	1*	1*	Н3	Н3	Н3		4	G1
	5	B2	B2	B2	K1	-	-	K2	-	-	VC-4 POH	5	F2
	6	D4	-	-	D5	-	-	D6	-	-		6	H4
STM-1 MSOH	7	D7	-	-	D8	-	-	D9	-	-		7	F3
	8	D10	-	-	D11	-	-	D12	-	-		8	K3
	9	Z1 (S1)	-	-	Z2	-	Z2 (M1)	E2	-	-		9	N1
	+: 10101010 -: undefined (NT1 -> LT: undefined LT -> NT1: don't care) Y: 1001SS11 (S bit is undefined.)												

1\*: 111111111

Figure 3-2/JJ-50.30 Mappings of overheads

Table 3-1/JJ-50.30 shows definitions of STM-1 SOH and AU-4 pointer. Table 3-2/JJ-50.30 shows definitions of VC-4 POH.

С	Overhead type	Function	Coding	Note	
	A1	Frame alignment	11110110	Complies with TTC JT-G707	
	A2	Frame alignment	00101000	Complies with TTC JT-G707	
RS	C1(J0)	Frame ID number	NT1 -> LT: 00000001 LT -> NT1: don't care	Complies with TTC JT-G707	
RSOH	B1	undefined	*		
	E1	undefined	*		
	F1	undefined	*		
	D1 - D3	undefined	*		
		AU-4 pointer		Complies with TTC JT-G707	
AU-4 pointer	H1, H2	Positive/negative stuffing indication	Prescribed coding	Complies with TTC JT-G707	
inter		P-AIS	H1=H2=1111111	Complies with TTC JT-G707	
	Н3	Pointer action	Negative stuffing	Complies with TTC JT-G707	
	B2	Error monitoring	BIP-24	Complies with TTC JT-G707	
	K1	undefined	*		
	K2 (b1 - b5)	undefined	*		
7	K2 (b6 - b8)	MS-RDI	Normal: 000 MS-RDI: 110	Complies with TTC JT-G707	
MSOH	D4 - D12	undefined	*		
	Z1 (S1)	undefined	*		
	Z2	R-INH, LOOP2	Refer to sections 4.3 and 4.4		
	Z2 (M1)	MS-REI (Section error reporting)	10000000 - 10011000: 0-24 errors 10011001 – 11111111: no error	Complies with TTC JT-G707	
	E2	undefined	*		

#### Table 3-1/JJ-50.30 Definitions of STM-1 SOH and AU-4 pointer

\* NT1 -> LT: undefined LT -> NT1: don't care

	Overhead type		Function	Coding	Note
	J1		Path trace	*	
	В3		Error monitoring	BIP-8	Complies with TTC JT-G707
	C2		Signal label	Prescribed coding	Complies with TTC JT-G707
	G1	(b1 - b4) P-REI		0000 - 1000: 0 - 8 errors 1001 - 1111: no error	Complies with TTC JT-G707
Р О Н		(b5)	P-RDI	0: normal 1: P-RDI	Complies with TTC JT-G707
Ĥ		(b6 - b8)	undefined	*	
	F2		undefined	*	
	H4		undefined	*	
	F3		undefined	*	
	K3		undefined	*	
	N1		undefined	*	

Table 3-2/JJ-50.30 Definitions of VC-4 POH

\* NT1 -> LT: undefined LT -> NT1: don't care

# 4. Transportation of maintenance and operation information

#### 4.1 Alarm transportation diagram

Figure 4-1/JJ-50.30 shows the alarm transportation diagram at the line interface.



(Note 1) The NT1 may not detect LOP, when it doesn't have pointer process.

(Note 2) MS-RDI generation in the case of detecting MS-SD is an option.

(Note 3) Since P-AIS generation in the case of detecting LOS, LOF, LOOP2 or LOP is an internal action of the NT1, this standard does not prescribe it. This figure shows an example.

Figure 4-1/JJ-50.30 Alarm transportation diagram

#### 4.2 Alarm detection and generation conditions

Table 4-1/JJ-50.30 shows the conditions of alarm detection and release, and Table 4-2/JJ-50.30 shows the conditions of alarm generation and release. Refer to sections 4.3 and 4.4 about R-INH and LOOP2.

Туре		Detection condition	Release condition	
Loss of input signal	LOS	Loss of input signal	Recovery of input signal	
Loss of frame alignment LOF		Detection of 5 successive inconsistent	Recovery of frame synchronization (Detection of 2 successive coincident frame synchronization pattern)	
Degradation of multiple section error rate	MS-SD		Transmission error rate detected by BIP-24 (B2) is less than 10 <sup>-7</sup> .	
Multiple section defect of transmitting side	MS-RDI	*	Receipt of 3 successive b6-b8 '110' in K2 after descramble	
Multiple section error of MS-ERR receiving side		Error detection by BIP-24 (B2)	No error detection by BIP-24 (B2)	
Multiple section error of transmitting side MS-REI		1	Detection of no transmission path error transported by M1	
Loss of pointer LOP		Receipt of abnormal pointer (except for receipt of AIS pointer)	Receipt of normal pointer	

Table 4-1/JJ-50.30 Conditions of alarm detection and release

Table 4-2/JJ-50.30 Conditions of alarm generation and release

Туре	Generation method	Generation condition	Release condition
MS-RDI	b6-b8='110' in K2 before scramble	Detection of LOS, LOF or (MS-SD)	Recovery of LOS, LOF or (MS-SD)
MS-REI	Put calculation result of B2 into M1	Detection of MS-ERR	Recovery of MS-ERR

#### 4.3 Power loss information bit of NT1 (R-INH)

An NT1 shall have the informing function of power loss in order to inhibit unnecessary alarms of the network side in the case of NT1 power loss.

R-INH bits are the 7th and the 8th bits of Z2 byte as shown in Figure 4-2/JJ-50.30.

When the NT1 power is on, the NT1 shall transmit R-INH bits of '00' to the LT. When the NT1 power is turned off from on (the power switch of the NT1 is turned off from on or the power supply is lost even if the power switch of the NT1 is on ), the NT1 shall transmit R-INH bits of '01' to the LT for 12 times and after that shall become signal loss state (except for the case of the

NT1 failures such as fuse burning ).

LT -> NT1

undefined	undefined	undefined	undefined	undefined	LOOP2	LOOP2	<b>'</b> 0'
b1	b2	b3	b4	b5	b6	b7	b8
						LOOP2-A	
undefined	undefined	undefined	undefined	undefined	LOOP2-A	СК	R-INH
undermed	undermed	undermed	undermed	undefined	СК	R-INH	K II (II
b1	b2	b3	b4	b5	b6	b7	b8
-> NT1		NT1	-> LT		NT1 -:	>LT	
b6 b7	LOOP2	b	7 b8	R-INH	b6	b7 I	LOOP2-ACK
<b>'</b> 00'	Set	ʻC	0'	Set	<b>'</b> 00	,	Set
·01'	Release	ʻC	1'	Release	'10	, I	Release
	b1 undefined b1 `-> NT1 b6 b7 '00'	b1 b2   undefined undefined   b1 b2   b1 b2   ···> NT1 ···   b6 b7 LOOP2   ·00' Set	b1 b2 b3 undefined undefined undefined b1 b2 b3 b1 b2 b3 $C \rightarrow NT1$ b2 b3 $C \rightarrow NT1$ $DOP2$ b5 OO' Set $OOP2$ $OP2$ $O$	b1 b2 b3 b4 undefined undefined undefined undefined $b1$ b2 b3 b4 b1 b4 b1 b2 b3 b4 b1 b4 b1 b2 b3 b4 b1 b4 b1 b2 b3 b4 b1 b4 b1 b4 b1 b4 b1 b2 b3 b4 b1 b4 b1 b4 b1 b4 b1 b4 b1 b2 b3 b4 b1 b4 b2 b4 b1 b4 b2 b4 b1 b4 b1 b4 b1 b4 b1 b4 b2 b4 b1 b4	b1 b2 b3 b4 b5 undefined undefined undefined undefined undefined $b1$ b2 b3 b4 b5 b1 b2 b3 b4 b5 2 > NT1 $b2$ b3 b4 b5 2 > NT1 $b2$ $b3$ $b4$ b5 2 > NT1 $b3$ $b4$ $b52 > NT1$ $b3$ $b4$ $b52 > NT1$ $b3$ $b4$ $b52 > NT1$ $b7$ $b8$ $R-INH2 > OO'$ $Set$	b1 b2 b3 b4 b5 b6 undefined undefined undefined undefined undefined undefined b1 b2 b3 b4 b5 b6 b1 b2 b3 b4 b5 b6 $\frac{1}{100}$ $\frac{1}{100}$ $\frac{1}{10$	b1 b2 b3 b4 b5 b6 b7 undefined undefined undefined undefined undefined b2 b3 b4 b5 b6 $CK$ b1 b2 b3 b4 b5 b6 b7 C > NT1 C > NT1 > LT C > NT1 > LT C > DOP2 + A + CK

(Note) The previous state shall be maintained in the case of receiving b6 and b7 bits of other than '00' or '01'.

Figure 4-2/JJ-50.30 Mappings of R-INH and LOOP2 into Z2 byte

#### 4.4 Loop information bit (LOOP2)

An NT1 shall have the loop back function (LOOP2) in order to perform effective identification of failure.

LOOP2 bits are the 6th and the 7th bits of Z2 byte as shown in Figure 4-2/JJ-50.30.

Table 4-3/ JJ-50.30 shows the loop back conditions and states of LOOP2.

#### Table 4-3/JJ-50.30 Loop back conditions and states

	Loop back condition	Loop back state
Set	Receipt of more than 6 successive LOOP2 bits of '01'	The NT1 transmits the signal (VC-4) received from the LT to the LT.
Release	Receipt of more than 6 successive LOOP2 bits of '00'	Loop back state is released and the NT1 returns to normal state.