TTC技術レポート
Technical Report

TR-G8271.1

「パケットネットワークにおける時刻同期に関するネットワーク限界」の技術レポート

Technical Report on Network limits for time synchronization in packet networks

第 1 版

2017 年 12 月 5 日制定

一般社団法人
情報通信技術委員会

THE TELECOMMUNICATION TECHNOLOGY COMMITTEE

目　次

I. パケットネットワークにおける時刻同期に関するネットワーク限界の技術レポート ..... - 4 -
1. はじめに ..... - 4 -
2. 調査報告概要 ..... - 4 -
3. 今後の進め方 ..... - 4 -
＜参考＞ ..... - 5 -
II. 概要説明 ..... - 6 -
III. 調査対象勧告和訳 ..... - 13 -

Ⅰ．パケットネットワークにおける時刻同期に関するネットワーク限界の技術レポート

1. はじめに

ITU-T においては、パケットネットワークにおけるネットワーク同期に関連する複数の勧告を発行している。モバイル通信網のバックボーン向けの技術としてパケットネットワークにおける同期技術が注目され、国際標準化や市場へのシステム導入が活発化している。TTC では、この様な背景を考慮し、関連する ITU-T 勧告の技術概要と翻訳を日本国内に広めることにより、本分野での産業界への貢献を目指している。本技術レポートでは ITU-T G.8271.1/Y.1366.1 勧告「パケットネットワークにおける時刻同期に関するネットワーク限界 Network limits for time synchronization in packet networks」の調査結果を報告する。

2. 調査報告概要

ITU-T G.8271.1/Y.1366.1 (10/2017) 勧告に相当する本技術レポート TR-G8271.1 では、フルタイミングサポートのパケットネットワークベースの時刻/位相同期に配信に関わる時刻/位相誤差に対する下記を規定

- ネットワーク限界
- 装置に対する最小雑音耐力
- ネットワーク機器に対する最低限必要な同期機能に関する概説

付録として Appendix I~IX が示されているが勧告としての強制力を持たないため、本文では和訳は提供せず ITU-T G.8271.1/Y.1366.1 (10/2017) 勧告の原文のままを示している。

3. 今後の進め方

モバイル通信網のバックボーンのアプリケーションとしてパケットネットワークでの同期技術が注目され、市場へのシステム導入や活発な国際標準化活動の背景から本勧告の調査を行った。今回調査を行った ITU-T G.8271.1/Y.1366.1 勧告はフルタイミングサポートのパケットネットワークベースの時刻/位相同期に配信に関わる時刻/位相誤差について規定している。しかし、技術的に発展途上であり、今後の 5G の導入、アプリケーションの進展などにより仕様変更の可能性があるため、今回は技術レポート化することにした。

＜参考＞

(1) 国際勧告等との関連

本技術レポートは ITU-T G.8271.1/Y.1366.1 (10/2017) を調査したものである。但し、Appendix I～IX は和訳せず、原文のままとしている。

(2) 上記国際勧告等に対する追加項目等

なし。

(3) 上記国際勧告等に対する変更事項

なし。

(4) 参照した国際勧告との章立て構成の相違

なし。

(5) 改版の履歴

版数	発行日	改版内容
第 1 版	2017 年 12 月 5 日	初版発行

(6) 工業所有権

本技術レポートに関わる「工業所有権等の実施の権利に係る確認書」の提出状況は、TTC ホームページでご覧になれます。

(7) その他、利用者に有益な事項

なし。

(8)標準作成部門

伝送網・電磁環境専門委員会

説明資料

TTC技術レポート概要報告

TR-G8271.1

「パケットネットワークにおける時刻同期に関するネットワーク限界」
の技術レポート

(Technical Report on Network limits
for time synchronization in packet networks)

一般社団法人情報通信技術委員会（TTC）
伝送網・電磁環境専門委員会（WG1300）
2017/12/5

1

はじめに

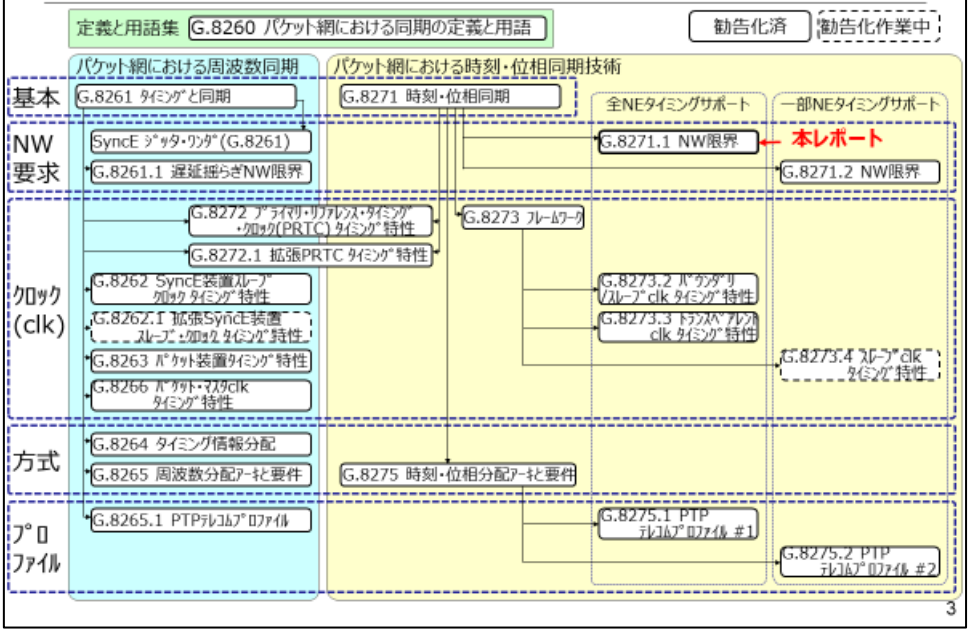
- ITU-Tにおいては、パケットネットワークにおけるネットワーク同期に関する複数の勧告(*1)を発行している。これらの勧告で標準化される同期技術はモバイル通信網のバックボーンのアプリケーションとして注目されている
- TTCにおいては、これらの勧告による技術の概要と翻訳を国内に広め、本分野での産業界への貢献を目指している
- 本技術レポートでは、PTPを用いたパケットベースの時刻/位相同期配信ネットワークにおけるネットワーク限界に関するITU-T G.8271.1/Y.1366.1勧告 (*2)「パケットネットワークにおける時刻同期に関するネットワーク限界」(Network limits for time synchronization in packet network)の調査結果を報告する

(*1) 2017年11月時点での勧告はITU-T G.8260, G.8261/Y.1361, G.8261.1/Y.1361.1, G.8262/Y.1362, G.8263/Y.1363, G.8264/Y.1364, G.8265, G.8265.1, G.8271/Y.1366, G.8271.1/Y.1366.1, G.8272/Y.1367, G.8273/Y.1368, G.8273.2/Y.1368.2, G.8273.3/Y.1368.3, G.8275/Y.1369, G.8275.1/Y.1369.1, G.8275.2/Y.1369.2, 詳細は本資料の3頁を参照。

(*2) 調査対象とした勧告はITU-T G.8271.1/Y.1366.1 (10/2017)

2

パケットネットワークでの同期技術関連勧告一覧



TR-G8271.1 目次構成

TR-G8271.1目次構成		（参考）ITU-T G.8271.1/Y.1366.1 Table of contents (10/2017)	
章	タイトル	Clause	Title
1	範囲	1	Scope
2	参照	2	References
3	定義	3	Definitions
3.1	他の勧告で定義されている用語	3.1	Terms defined elsewhere
3.2	本勧告で定義されている用語	3.2	Terms defined in this Recommendation
4	略語および頭字語	4	Abbreviations and acronyms
5	慣例	5	Conventions
6	ネットワーク参照モデル	6	Network reference model
7	ネットワーク限界	7	Network limits
7.1	参照点Aでのネットワーク限界	7.1	Network limits at reference point A
7.2	参照点Bでのネットワーク限界	7.2	Network limits at reference point B
7.3	参照点Cでのネットワーク限界	7.3	Network limits at reference point C
7.4	参照点Dでのネットワーク限界	7.4	Network limit at reference point D
7.5	参照点Eでのネットワーク限界	7.5	Network limit at reference point E
注）ITU-T G.8271.1/Y.1366.1 (10/2017)勧告のAppendixは参考情報であり強制力のある勧告とはみなされないので本TRでの報告の対象外とした		Appendix I	Clock models for noise accumulation simulations
		Appendix II	HRMs used to derive the network limits
		Appendix III	Network limits considerations
		Appendix IV	Constant and dynamic time error and error accumulation
		Appendix V	Example of design options
		Appendix VI	Mitigation of time error due to synchronous Ethernet transients
		Appendix VII	Maximum relative time error
		Appendix VIII	Models for Budgeting in a chain of Microwave Devices
		Appendix IX	Models for Budgeting in a chain of xPON or xDSL Devices

4

第１章 Scope – 本勧告が対象とする領域

PTPを用いたフルタイミングサポートのパケットネットワークベースの時刻/位相同期配信に関して、時刻/位相誤差に対するネットワーク制限を規定する

G.8271.1/Y.1366.1勧告の2017/10版では、フルタイミングサポートのパケットネットワークベースの時刻/位相同期に配信に関わる時刻/位相誤差に対する下記を規定

- ネットワーク限界
- 装置に対する最小雑音耐力
- ネットワーク機器に対する最低限必要な同期機能に関する概説

ネットワークからのプロトコルレベルでフルタイミングサポートする方式に基づくパケットベースのネットワークに渡る時刻と位相配信の場合について取り組む

なお、物理レイヤは[IEEE 802.3-2005]で定義されるEthernet media typeとなる

5

第5章 慣例

本勧告中では下記の慣例を用いる

- PTP (Precision Time Protocol):
  IEEE 1588で規定されるPTP version 2(*) プロトコルを指す
- dynamic time error and time noise:
  タイミング信号のジッタとワンダ成分を示すものとして区別しないで用いる

(*) IEEE 1588-2008版

6

第6章 ネットワーク参照モデル

一般的なネットワーク参照モデルは [ITU-T G.8271] の中で述べられている。

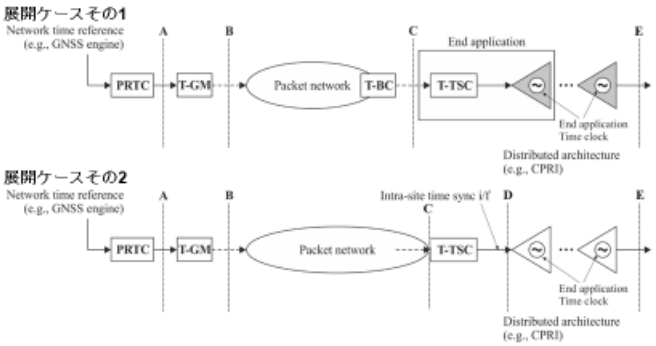
- 注: 本文中では、ITU-T G.8271への参照のみが記載されており、具体的な規格については述べられていない

7

第7章 ネットワーク限界

2つのメインシナリオが想定され、関連するネットワーク限界の定義の中で考慮される

- 展開ケース その1: エンドアプリケーションの中に統合されているT-TSCと配信アーキテクチャを持つエンドアプリケーションを含む時刻配信チェーン。
  T-TSCの性能特性は[ITU-T G.8273.2]のスコープ外。
- 展開ケース その2: エンドアプリケーションの外にあるT-TSCと配信アーキテクチャを持つエンドアプリケーションを含む時刻配信チェーン。
  T-TSCの性能特性は[ITU-T G.8273.2]において定義。



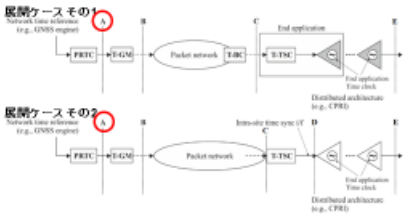
8

第7.1節 参照点Aにおけるネットワーク限界

- 参照点A (PRTC の出力) でのネットワーク限界は [ITU-T G.8272] で定義
- 具体的に、最大絶対時刻誤差(max |TE|)は次式で定義

  $|TE| \leq 100$ ns

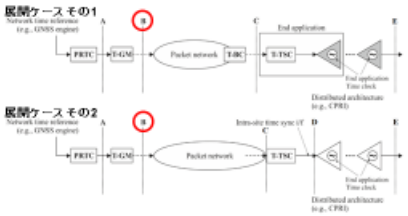
- 参照点Aで適用可能なダイナミック時刻誤差ネットワーク限界も [ITU-T G.8272] において規定される。



9

第7.2節 参照点Bにおけるネットワーク限界

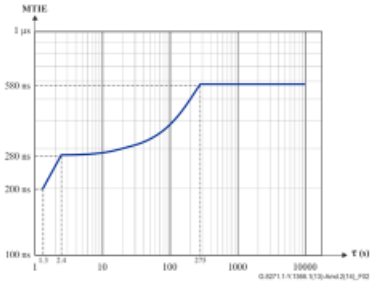
- PRTCに統合されたT-GM の場合
  参照点Bにおいて適用可能なネットワーク限界は参照点Aでの限界と同じ
- PRTCに含まれないT-GMの場合
  参照点Bで適用できるネットワーク限界は今後の検討課題



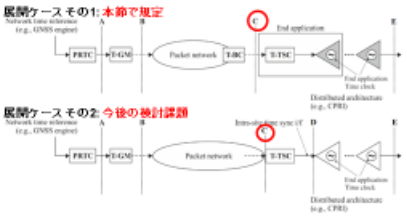
10

第7.3節 参照点Cにおけるネットワーク限界

- 本節では、[ITU-T G.8271]表1に示すクラス4に対応するアプリのネットワーク限界を規定
  その他のクラスについては今後の検討課題
- 展開ケース その1に対する規定
  - 最大絶対時刻誤差限界は以下で規定
    max |TE| ≤ 1‘100 ns
  - ダイナミック低周波数時刻誤差ネットワーク限界は下記に示すMTIEで規定



- 展開ケース その2に対する規定
  - 今後の検討課題

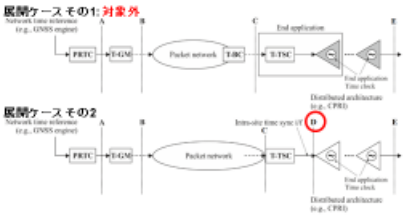


11

第7.4節 参照点Dにおけるネットワーク限界

- 展開ケース その1でのネットワーク限界
  今後の検討課題

- 展開ケース　その2でのネットワーク限界
  参照点Dでのネットワーク限界は、展開ケース その1の参照点Cでのネットワーク限界と同じ

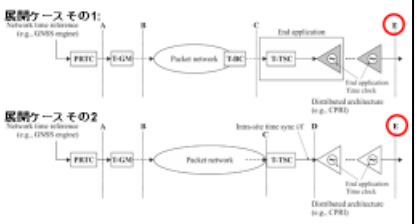


12

第7.5節 参照点Eにおけるネットワーク限界

- 参照点Eにおいて適用されるネットワーク限界
  [ITU-T G.8271] 表1において定義される特定のアプリケーションによって定義

  本勧告では[ITU-T G.8271]表1に示されるクラス4，5, 6に対するアプリケーションが考慮されている



13

TR-G8271.1 調査結果まとめ

- 本報告で調査を行ったITU-T G.8271.1/Y.1366.1勧告はフルタイミングサポートのパケットネットワークベースの時刻/位相同期に配信に関わる時刻/位相誤差に対するネットワーク限界について規定しており、装置の実装のために重要な技術である。

  しかし、技術的に発展途上であり、今後の5Gの導入、アプリケーションの進展などにより仕様変更の可能性があるため、今回は技術レポート化することにした。

14

Ⅲ．調査対象勧告和訳

ITU-T G.8271.1/Y.1366.1勧告

パケットネットワークにおける時刻同期に関するネットワーク限界

概要

ITU-T G.8271.1/Y.1366.1 は超過してはならない位相と時刻の誤差に対する最大のネットワーク限界を規定する。位相と時刻の同期インタフェースでのパケットネットワークの境界において提供される位相と時刻の誤差に対する最小装置耐力を規定する。また、ネットワーク機器の同期機能に対する最小限の要求について概略を述べる。

本勧告はネットワークからのプロトコルレベルでフルタイミングサポートする方式に元づくパケットベースのネットワークに渡る時刻と位相配信の場合について取り組む。

キーワード

同期、時刻、位相、フルタイミングサポート、ネットワーク限界、高精度タイム・プロトコル

改版履歴

Edition	Recommendation	Approval	Study Group	Unique ID*
1.0	ITU-T G.8271.1/Y.1366.1	2013-08-29	15	11.1002/1000/12034
1.1	ITU-T G.8271.1/Y.1366.1 (2013) Amd. 1	2014-05-14	15	11.1002/1000/12194
1.2	ITU-T G.8271.1/Y.1366.1 (2013) Amd. 2	2015-01-13	15	11.1002/1000/12392
2.0		2017-10-07	15	

* To access the Recommendation, type the URL http://handle.itu.int/ in the address field of your web browser, followed by the Recommendation's unique ID. For example, http://handle.itu.int/11.1002/1000/11830-en.

目次

1　範囲 - 15 -
2　参照 - 15 -
3　定義 - 16 -
3.1 他の勧告で定義されている用語 - 16 -
3.2 本勧告で定義されている用語 - 16 -
4　略語および頭字語 - 16 -
5　慣例 - 17 -
6　ネットワーク参照モデル - 17 -
7　ネットワーク限界 - 17 -
7.1 参照点 A におけるネットワーク限界 - 18 -
7.2 参照点 B におけるネットワーク限界 - 18 -
7.3 参照点 C におけるネットワーク限界 - 18 -
7.4 参照点 D におけるネットワーク限界 - 20 -
7.5 参照点 E におけるネットワーク限界 - 20 -
APPENDIX I　CLOCK MODELS FOR NOISE ACCUMULATION SIMULATIONS - 21 -
I.1 T-BC MODELS FOR NOISE ACCUMULATION SIMULATIONS - 21 -
I.2 END-TO-END TC MODELS FOR NOISE ACCUMULATION SIMULATIONS - 23 -
APPENDIX II　HRMS USED TO DERIVE THE NETWORK LIMITS - 26 -
II.1 HRM COMPOSED OF T-BCS - 26 -
II.1.1　HRM without physical layer frequency support from the network - 26 -
II.1.2　HRM with physical layer frequency support from the network - 27 -
II.1.3　HRM for cluster-based synchronization - 30 -
II.2 HRM COMPOSED OF T-BCS AND T-TCS - 31 -
II.2.1　HRM with physical layer frequency support from the network - 31 -
APPENDIX III　NETWORK LIMITS CONSIDERATIONS - 32 -
III.1 MEASUREMENT OF NETWORK LIMITS IN CASE OF DEPLOYMENT CASE 1 - 32 -
APPENDIX IV　CONSTANT AND DYNAMIC TIME ERROR AND ERROR ACCUMULATION - 34 -
IV.1 INTRODUCTION - 34 -
IV.2 COMPONENTS OF TIME ERROR - 34 -
IV.3 ACCUMULATION OF TIME ERROR IN A CHAIN OF CLOCKS - 34 -
APPENDIX V　EXAMPLE OF DESIGN OPTIONS - 37 -
V.1 NETWORK LIMITS - 37 -
V.2 COMPONENTS OF TIME ERROR BUDGETS - 37 -
V.3 FAILURE SCENARIOS - 37 -
V.4 TIME ERROR BUDGET ALLOCATION - 38 -
V.5 OPERATOR OPTIONS - 39 -
V.6 FURTHER DETAILS - 39 -
APPENDIX VI　MITIGATION OF TIME ERROR DUE TO SYNCHRONOUS ETHERNET TRANSIENTS - 42 -
APPENDIX VII　MAXIMUM RELATIVE TIME ERROR - 43 -
FIGURE VII.1 – ILLUSTRATION OF RELATIVE TIME ERROR - 43 -
APPENDIX VIII　MODELS FOR BUDGETING IN A CHAIN OF MICROWAVE DEVICES - 45 -
APPENDIX IX　MODELS FOR BUDGETING IN A CHAIN OF XPON OR XDSL DEVICES - 48 -

ITU-T G.8271.1/Y.1366.1 勧告

ネパケットネットワークにおける時刻同期に関するネットワーク限界

1　範囲

ITU-T G.8271.1/Y.1366.1 は超過してはならない位相と時刻の誤差に対する最大のネットワーク限界を規定する。位相と時刻の同期インタフェースでのパケットネットワークの境界において提供される位相と時刻の誤差に対する最小装置耐力を規定する。また、ネットワーク機器の同期機能に対する最小限の要求について概略を述べる。

本勧告はネットワークからのプロトコルレベルでフルタイミングサポートする方式に基づくパケットベースのネットワークに渡る時刻と位相配信の場合について取り組む。

本規定に関連する物理レイヤは [IEEE 802.3-2005] で定義される Ethernet media type である。

2　参照

以下の ITU-T 勧告と参考文献は本文中での参照を通して、本勧告の規定を構成する規定を含む。出版時においては、以下に示された版が有効である。全勧告と他の参考文献は改訂される。従って、本勧告の読者は以下の勧告と参考文献の最新版の適用の可能性を調査することを推奨する。現在有効な ITU-T 勧告の一覧は正規に発行されている。

本勧告内の文章での参照は独立した文章としてその勧告に地位を与えるものではない。

[ITU-T G.803]　Recommendation ITU-T G.803 (2000), *Architecture of transport networks based on the synchronous digital hierarchy (SDH)*.

[ITU-T G.810]　Recommendation ITU-T G.810 (1996), *Definitions and terminology for synchronization networks*.

[ITU-T G.812]　Recommendation ITU-T G.812 (2004), *Timing requirements of slave clocks suitable for use as node clocks in synchronization networks*.

[ITU-T G.823]　Recommendation ITU-T G.823 (2000), *The control of jitter and wander within digital networks which are based on the 2048 kbit/s hierarchy*.

[ITU-T G.8260]　Recommendation ITU-T G.8260 (2015), *Definitions and terminology for synchronization in packet networks*.

[ITU-T G.8262]　Recommendation ITU-T G.8262/Y.1362 (2015), *Timing characteristics of a synchronous Ethernet equipment slave clock.*

[ITU-T G.8271]　Recommendation ITU-T G.8271/Y.1366 (2016), *Time and phase synchronization aspects of packet networks*.

[ITU-T G.8272]　Recommendation ITU-T G.8272/Y.1367 (2015), *Timing characteristics of primary reference time clocks*.

[ITU-T G.8273]　Recommendation ITU-T G.8273/Y.1368 (2013), *Framework of phase and time clocks*.

[ITU-T G.8273.2]　Recommendation ITU-T G.8273.2/Y.1368.2 (2017), *Timing characteristics of telecom boundary clocks and telecom time slave clocks*.

[ITU-T G.8275]　Recommendation ITU-T G.8275/Y.1369 (2013), *Architecture and requirements for packet-based time and phase distribution*.

[IEEE 802.3-2015]　IEEE 802.3-2015, IEEE Standard for Ethernet

<http://standards.ieee.org/getieee802/802.3.html>.

[IEEE 1588-2008] IEEE 1588-2008, *Standard for a Precision Clock Synchronization Protocol for Networked Measurement and Control Systems*.
http://standards.ieee.org/findstds/standard/1588-2008.html

3 定義

3.1 他の勧告で定義されている用語

本勧告は、他の勧告で定義された以下の用語を用いる：

本勧告で用いられる用語と定義は [ITU-T G.810] および [ITU-T G.8260] に含まれる。

3.2 本勧告で定義されている用語

なし。

4 略語および頭字語

本勧告は下記の略語および頭字語を用いる。

EEC	Synchronous Ethernet Equipment Clock 同期イーサネット機器クロック
GNSS	Global Navigation Satellite System 全地球的航法衛星システム
HRM	Hypothetical Reference Model 仮説に基づいた参照システム
LTE	Long Term Evolution ロング・ターム・エボリューション
MTIE	Maximum Time Interval Error 最大時間間隔誤差
PHY	Physical layer 物理レイヤ
PLL	Phase-Locked Loop 位相同期ループ
PPS	Pulse Per Second パルス/秒
PRTC	Primary Reference Time Clock プライマリ・リファレンス・タイム・クロック
PTP	Precision Time Protocol 高精度タイム・プロトコル
SDH	Synchronous Digital Hierarchy 同期デジタル・ハイアラーキ
SSM	Synchronization Status Message 同期状態メッセージ
SSU	Synchronization Supply Unit 同期供給ユニット
TDEV	Time DEViation 時刻偏差
TDD	Time Division Duplex

	時分割二重化
TE	Time Error
	時刻誤差
T-BC	Telecom Boundary Clock
	テレコム・バウンダリ・クロック
T-GM	Telecom Grand Master
	テレコム・グランドマスタ
T-TC	Telecom Transparent Clock
	テレコム・トランスペアレント・クロック
T-TSC	Telecom Time Slave Clock
	テレコム・タイム・スレーブ・クロック

5　慣例

本勧告内では、次の慣例が用いられる。用語”高精度タイム・プロトコル (PTP) ”は [IEEE 1588-2008] において定義される PTP プロトコルを参照する。

用語”ダイナミック時刻誤差および時刻雑音”は本勧告のあらゆる場所で、タイミング信号のジッタとワンダ成分を示すものとして区別しないで用いられる。

6　ネットワーク参照モデル

一般的なネットワーク参照モデルは [ITU-T G.8271] の中で述べられている。

7　ネットワーク限界

下記のメインシナリオ (すなわち最悪ケース) が想定され、関連するネットワーク限界の定義の中で考慮される。

- 展開ケース その 1: エンドアプリケーションの中に統合されているテレコム・タイム・スレーブ・クロック (T-TSC) と配信アーキテクチャを持つエンドアプリケーションを含む時刻配信チェーン。この場合、T-TSC の性能特性は [ITU-T G.8273.2] のスコープ外である。
- 展開ケース その 2: エンドアプリケーションの外にある T-TSC と配信アーキテクチャを持つエンドアプリケーションを含む時刻配信チェーン。注: 特定の装置実装は (T-TSC 機能の代わりに) テレコム・バウンダリ・クロック (T-BC) 、かつ、位相/時刻同期配信インタフェースを介してエンドアプリケーションに位相/時刻基準を配達するものを元にする装置であるかもしれない。この場合、T-TSC の性能特性は [ITU-T G.8273.2] において定義される。

展開ケースは図 7-1 に示される。

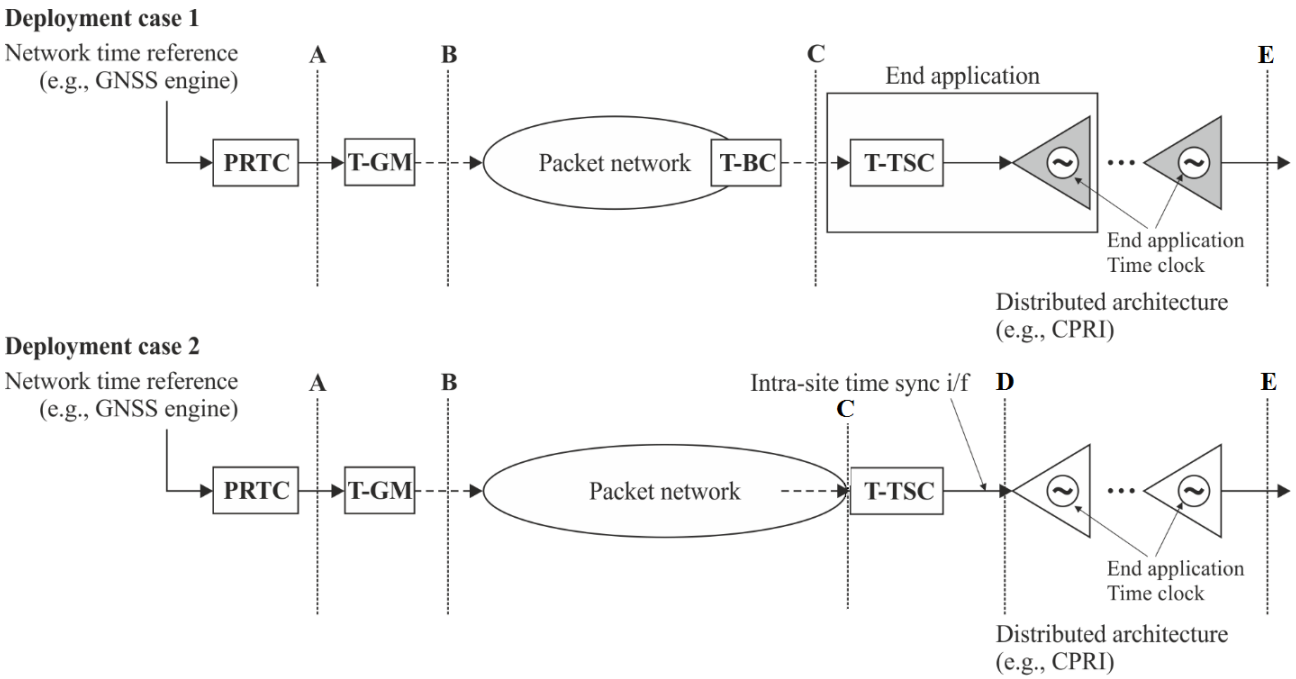


図 7-1 － 時刻同期展開ケース

注 － 配信アーキテクチャの例は基地局が無線ユニット (無線装置 (RE) とも呼ばれる) に遠隔で接続されているベースバンドユニット (無線装置制御 (REC) とも呼ばれる) を持つモバイルアプリケーションの場合である。この場合、ポイント・ツー・ポイント (例、ファイバを介して) が仮定され、チェーントポロジが可能である。この接続に適用できる時刻誤差 (TE) バジェットは 150ns と想定されるが、チェーントポロジの詳細は今後の検討課題である。

7.1 参照点 A におけるネットワーク限界

参照点 A、すなわち、プライマリ・リファレンス・タイム・クロック (PRTC) の出力で、適用可能なネットワーク限界は [ITU-T G.8272] で定義される。具体的には、[ITU-T G.8272] によると、最大絶対時刻誤差は次のとおりとなる。

$|TE| \leq 100$ ns

注 － 本限界は通常の時刻同期している状況下で適用できる。PRTC における障害状態での本限界については今後の検討課題である。

参照点 A で適用可能なダイナミック時刻誤差ネットワーク限界も [ITU-T G.8272] において規定される。

7.2 参照点 B におけるネットワーク限界

PRTC に統合されたテレコム・グランドマスタ (T-GM) の場合、参照点 B において適用可能なネットワーク限界は参照点 A で適用できる限界と同じである。

PRTC に含まれない T-GM の場合、参照点 B で適用できるネットワーク限界は今後の検討課題である。

7.3 参照点 C におけるネットワーク限界

本節で与えられる限界は、[ITU-T G.8271] の表 1 に示されるクラス 4 に対応するアプリケーションに従った位相/時刻同期の配信を担うパケットネットワーク内のインタフェースにおける位相/時刻誤差と雑音の最大許容レベルを示している。

参照点 C での他のクラスに適用可能な限界は今後の検討課題である。

T-BC チェーンによって生成される雑音は次に示す 2 つの主な観点で特徴付けられる:

1. チェーンによって発生する一定の時刻誤差であり、例えば、(PRTC を含む) 様々な固定要因や補償されなかった非対称性に起因するものである。

2. (PRTC を含む) 様々な構成要素によって発生するダイナミックな時刻誤差。この雑音は低周波数または高周波数雑音として分類され、それぞれ 0.1Hz 以下または 0.1Hz 以上の成分に対応する。

参照点 C において適用できるネットワーク限界は 2 つの量を単位として表現される。

1. 最大絶対時刻誤差: max |TE|、ここでは一定時刻誤差およびダイナミック時刻誤差の低周波数成分を含んでいる。
2. ダイナミック時刻誤差に適用される適切な測定基準 (特に、MTIE および TDEV が 0.1Hz よりも低い周波数を持つ雑音成分の測定に用いられる。また、peak-to-peak TE は 0.1Hz よりも高い周波数をもつ雑音成分の測定に用いられる。)

インタフェースに先行する機器の量に関係なく、下記で与えられる限界は全てのオペレーション状態に対して満たすべきである (ネットワークの中の PTP 再構成時と長期のホールドオーバ状態の間、また、今後の検討課題である PTP および物理レイヤの周波数再設定の状態の間を除く。Appendix V に示す例を参照) 。一般的には、これらネットワーク限界は、全装置の入力ポートが提供することを要求される時刻誤差と雑音に対する最小耐力に等しい。位相/時刻配信ネットワークをどのように設計するかの更なる手引き書は本勧告の Appendix V において提供される。

展開ケース その 1 に対する、参照点 C で適用可能なネットワーク限界は下記のとおりである。

- 最大絶対時刻誤差限界、max |TE| ≤ 1'100 ns.
- ダイナミック低周波数時刻誤差ネットワーク限界: MTIE を単位とするこの規定は表 7-1 と図 7-2 に示される。TDEV を単位とするこの規定は今後の検討課題である。

表 7-1 - MTIE で表現されたダイナミック時刻誤差ネットワーク限界

MTIE 限界 (ns)	測定間隔, τ (s)
100 + 75τ	1.3 < τ ≤ 2.4
277 + 1.1τ	2.4 < τ ≤ 275
580	275 < τ ≤ 10'000

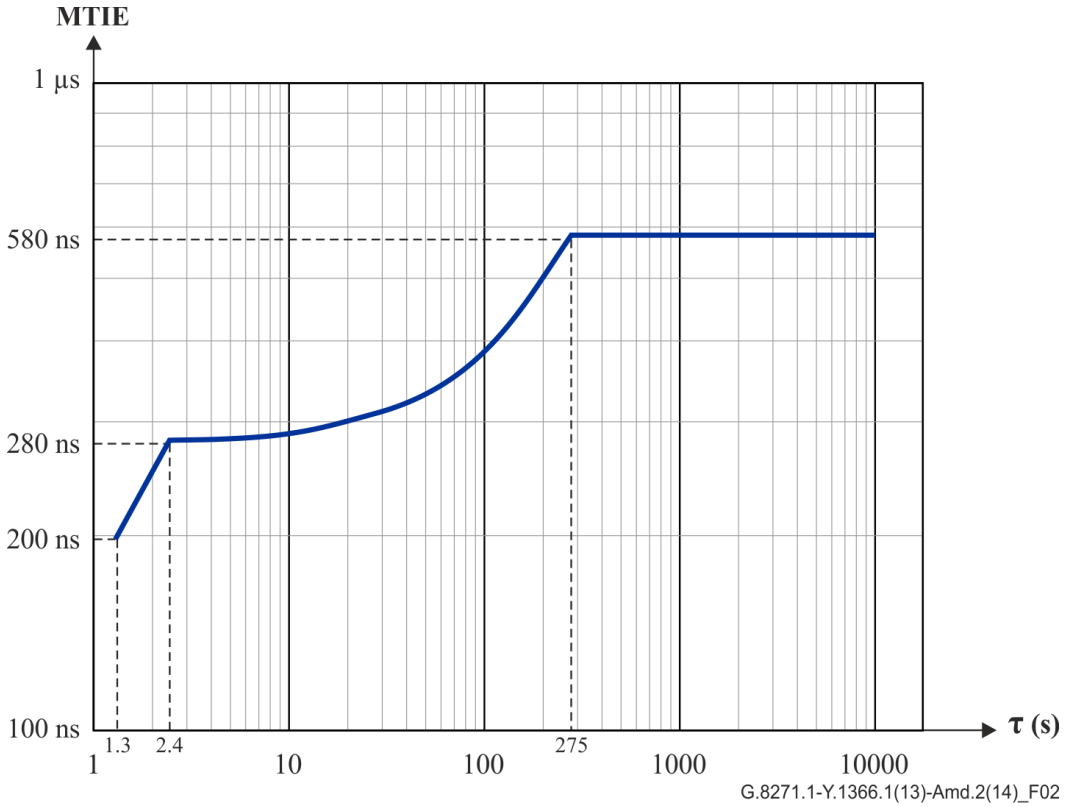


図 7-2 - ダイナミック時刻誤差ネットワーク限界 (MTIE)

帯域幅 0.1Hz の 1 次ローパス測定フィルタが max |TE|、MTIE および TDEV を評価する前のパケットタイミングインタフェースで測定される TE サンプルに適用される。また、1PPS テスト出力で行われるネットワーク限界の測定は 1PPS 信号に同様にフィルタを行うべきである。

試験装置特性や測定周期に関する追加の詳細もまた、今後の検討課題である。

注 - 上記の MTIE 規定は大量のコンサバな仮定が適用された結果であり、理論的には、300ns 以上の max |TE|と 0.1Hz 以下の周波数成分を持つダイナミック成分により導き出される。しかしながら、本勧告および [ITU-T G.8273.2] などの他の関連する勧告においての仮定では、関連するダイナミック雑音成分が常に 300ns 以下の max |TE|となることが実証されている。

10,000 秒を超える間隔での測定において、0.1Hz よりも高い周波数成分に対して次の要求が適用される (パケットタイミングインタフェースで測定される TE サンプル、または、1PPS 信号に対して帯域幅 0.1Hz の 1 次ハイパスフィルタが適用されるべきである。)

- peak-to-peak TE amplitude < 200 ns

展開ケース その 2 に対して、参照点 C で適用可能なネットワーク限界は今後の検討課題である。

7.4 参照点 D におけるネットワーク限界

展開ケースその 1 では、参照点 D はアクセスできない可能性がある。参照点 D におけるネットワーク限界は、今後の検討課題である。

展開ケースその 2 では、参照点 D におけるネットワーク限界は、7.3 節に記載されている展開ケースその 1 の参照点 C のネットワーク限界と同じである。

7.5 参照点 E におけるネットワーク限界

参照点 E において適用されるネットワーク限界は、 [ITU-T G.8271] 表 1 において定義される特定のアプリケーションによって定義される。

[ITU-T G.8271] 表 1 に従うと、現在のところ、クラス 4, 5, 6 に対応するアプリケーションが本勧告において考慮されている。

Appendix I

Clock models for noise accumulation simulations

(This appendix does not form an integral part of this Recommendation.)

Simulations are needed to define limits on the various noise types described in [ITU-T G.8271]. To perform these simulations, a simulation model that shows how to simulate each noise type it introduces into the timing signal needs to be defined for each network element participating in the time distribution scheme.

I.1 T-BC models for noise accumulation simulations

This clause describes T-BC models for simulating the transport of time using PTP and frequency using synchronous Ethernet and a T-BC model for simulating the transport of both time and frequency using PTP.

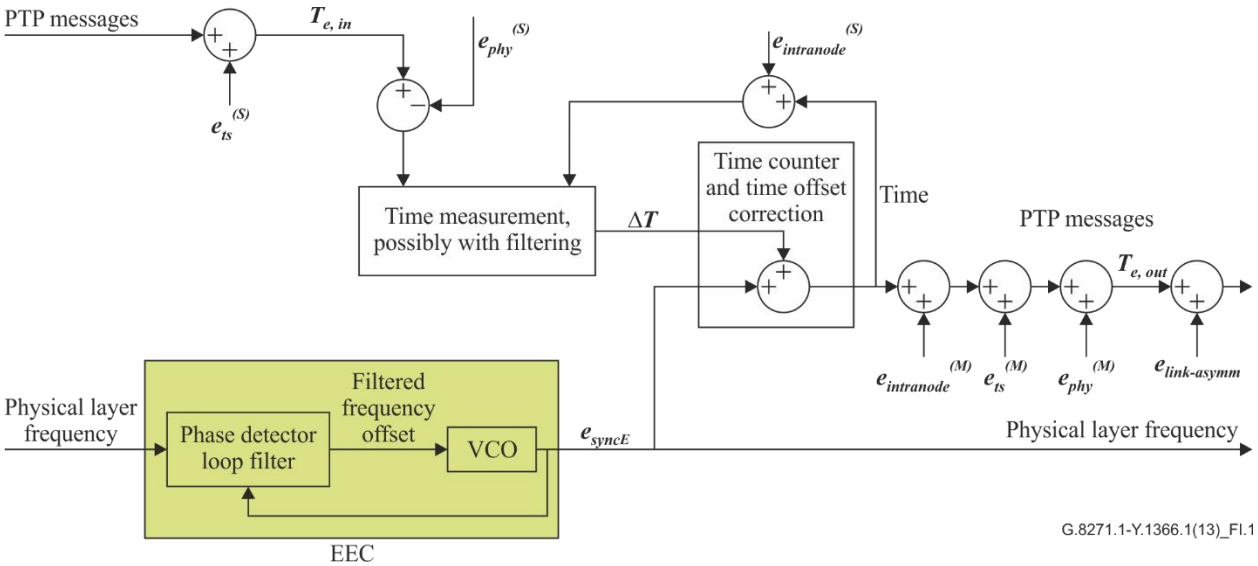


Figure I.1 – Telecom boundary clock model for simulating the transport of time using PTP with synchronous Ethernet assistance

Figure I.1 illustrates a model for simulating the transport of time using PTP with synchronous Ethernet assistance.

NOTE – This model, used for the evaluation of a worst-case noise accumulation when synchronous Ethernet is combined with PTP, may not be representative of all possible implementations.

The synchronous Ethernet equipment clock (EEC) block represents an Ethernet equipment clock, as specified in [ITU-T G.8262]. The EEC input is a physical layer frequency (i.e., a physical layer signal that is used as a frequency reference), and its output is a local frequency (i.e., a physical layer signal that has a frequency and is local to this node) that is optionally propagated to downstream nodes. The noise process, $e_{syncE,}$ represents the synchronous Ethernet phase noise accumulation in the synchronous Ethernet hypothetical reference model (HRM) (see Appendix II).

The time counter (TC) is incremented by the nominal period of the output clock of the EEC block. For example, if the output clock rate is 125 MHz, then the time counter is incremented by 8 ns each rising edge of the synchronous Ethernet output clock. Upon reception and transmission of a PTP event messages, the time counter is sampled. The difference between the actual transmission/reception time and the sampled value of the time counter is modelled as, $e_{ts,}$ since the transmission/reception event can happen between two rising edges of this clock. The effect of e_{ts} on the timestamp for reception of a PTP event message is shown added at the input, and the effect of e_{ts} on the timestamp for transmission of a PTP event message is shown added at the output.

The incoming PTP messages contain information that may be used to obtain an estimate of the grandmaster (i.e., PRTC) time. This estimate is not perfect; it contains errors introduced by the grandmaster, the upstream nodes, and upstream links. The error in the incoming estimate of the grandmaster time is represented by $T_{e,in}$. The noise process, $e_{phy,}$ represents the effect of asymmetry and timestamp sampling uncertainty on the physical layer (PHY) of the input port. The PHY latency asymmetry may be present if timestamping is done at a point other than the reference plane (i.e., the interface between the PHY and the physical medium). Any latency between the point where timestamping actually is done and the reference plane may be compensated for within PTP. However, any uncompensated latencies that result in asymmetry will contribute to e_{phy}. The noise e_{phy} is subtracted from the timing information

contained in the incoming PTP messages due to the direction of the time distribution (note, that on the master port of the T-BC it is added). Note that the random process, $e_{phy,}$ may have a static component and a time-varying component.

The timing information contained in the incoming PTP messages, with the noise due to asymmetry on the input port PHY, e_{phy}, and the timestamping error, e_{ts}, is input to the block labelled time measurement, possibly with filtering. This block compares the local time output of the local clock, which is the accumulation of the syncE phase noise, $e_{syncE,}$ and the prior time offset correction, ΔT, with the timing input that represents an estimate of the grandmaster time (with errors as described in the previous paragraph). This block produces the time offset correction, ΔT, between the grandmaster time estimate and the local time. The time measurement block might provide filtering when computing the time offset correction, to reduce the effect of the short-term noise in the observed time error. The filtering characteristics are for further study.

The time counter and time offset correction block produces a local time output (i.e., the output labelled "time"). The input to the time counter and time offset correction block is the output of the EEC and the time offset correction of the time measurement block. The counter and time offset correction block may include a low-pass filtering function. This has the same effect as increasing the output frequency of the EEC block.

The local time is sampled upon transmission and reception of PTP event messages on master ports. The sampled value is the accumulation of the synchronous Ethernet phase noise, e_{syncE}, the timestamp error, e_{ts}, and the offset correction, ΔT. The error due to asymmetry of the PHY on the output port, e_{phy}, is added to the sampled local time to produce the master port output time error, $T_{e,out}$. The quantity, $T_{e,out}$, is input to the next PTP node (T-BC or telecom time slave clock (T-TSC)) downstream via a link model.

Errors due to intranode transmission, $e_{intranode}$, and link asymmetry, $e_{link\text{-}asymm}$, must also be included. The former affects both the time correction and the T-BC output. The latter is shown added to the output of the T-BC.

Figure I.2 describes an equivalent model suitable for analytical studies.

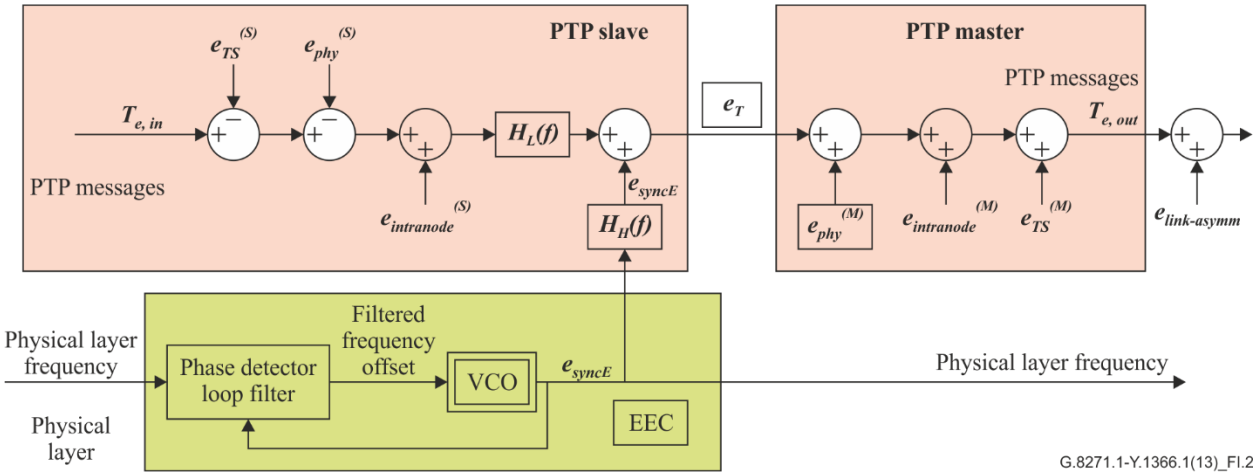
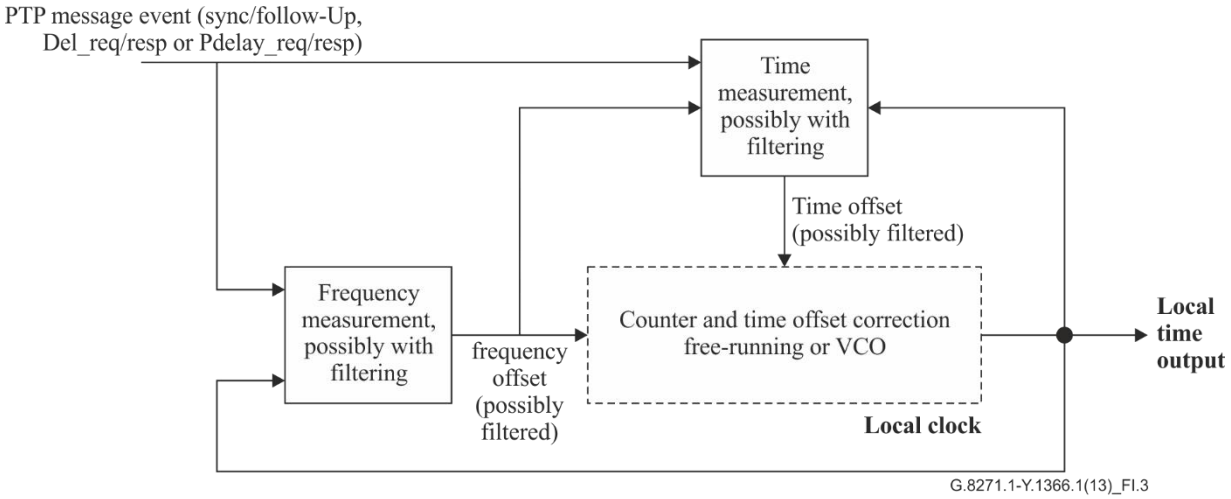


Figure I.2 – Telecom boundary clock model for analytical studies of the transport of time using PTP with synchronous Ethernet assistance

In Figure I.2 the slave clock is assumed to have time error filtering indicated by the low-pass filter $H_L(f)$. The physical layer clock noise experiences a high-pass characteristic, $H_H(f)$. When there is no time error filtering the physical layer clock introduces a time error corresponding to the wander (e_{syncE}) that occurs between successive estimates of the time offset correction.

The following figure describes a model using PTP for time and frequency. The details for this model are for further study.



NOTE – The ingress and egress hardware timestamping needs to be modelled and taken into account.

Figure I.3 – Telecom boundary clock model using PTP for time and frequency

In Figure I.3:

- PTP messages are used for both frequency and time measurements. The PTP messages are timestamps based on the local time output.
- The frequency measurement block uses PTP messages to make frequency measurements. For frequency measurements there are several possibilities (e.g., Sync or Pdelay_req messages) and these are for further study. The frequency measurements could involve filtering and is for further study. The PTP messages are timestamps based on the local time output.
- The time measurement block uses PTP messages for computing a time offset; this block should consider sources of errors such as the effect of timestamping. The PTP messages are timestamps based on the local time output. The time measurement block might provide filtering, for example, to reduce the effect of the error produced by the timestamping function. The filtering characteristics are for further study.
- The local clock block includes a counter to produce a local timebase output. The input into this block is a frequency measurement from the frequency measurement block and a time correction from the time measurement block. The ways in which these are used is for further study.

For the simulation model using PTP for time and frequency, it can be assumed that filtering is implemented in each boundary clock with a phase-locked loop (PLL)-based clock.

I.2 End-to-end TC models for noise accumulation simulations

This section describes models for simulating the noise added by a PTP transparent clock when using synchronous Ethernet or a free running local oscillator (see [IEEE 1588-2008] for details on the transparent clock functions). The models for the case where PTP is the source for frequency reference are for further study.

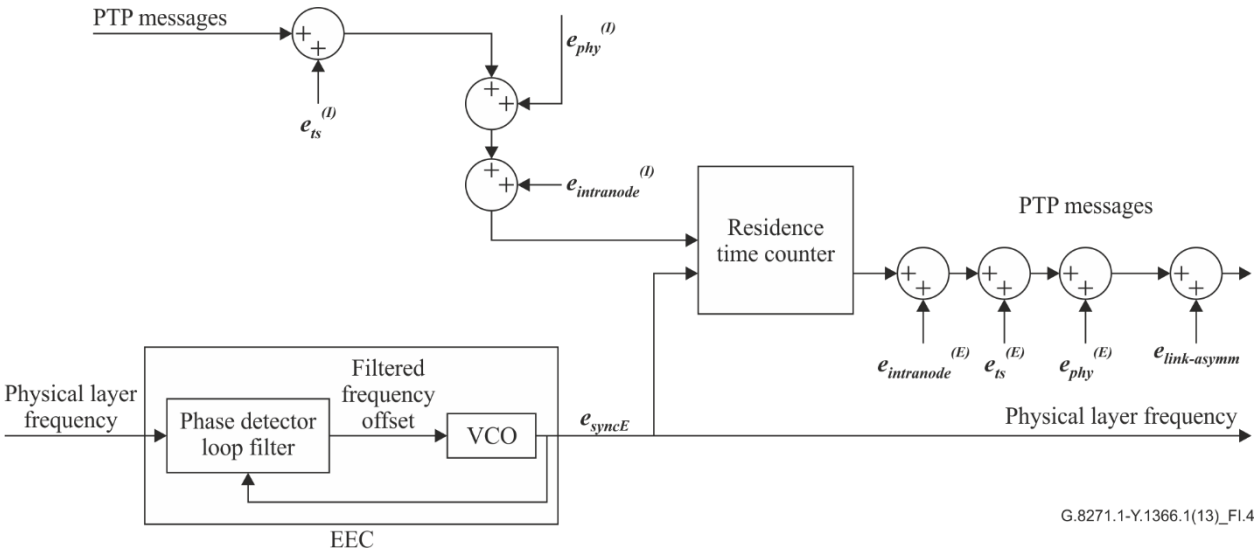


Figure I.4 – Telecom end-to-end transparent clock model for simulating the transport of time using PTP with synchronous Ethernet assistance

Figure I.4 illustrates a model for simulating the transport of time using PTP with optional synchronous Ethernet assistance for the case of an end-to-end transparent clock.

NOTE 1 – This model, used for the evaluation of a worst-case noise accumulation when synchronous Ethernet is combined with PTP, may not be representative of all possible implementations.

NOTE 2 – This model accounts for the noise added by the end-to-end transparent clock to the PTP flow in one direction only. End-to-end transparent clocks operate independently of the PTP traffic flow direction.

The EEC block represents an Ethernet equipment clock, as specified in [ITU-T G.8262]. The EEC input is a physical layer frequency (i.e., a physical layer signal that is used as a frequency reference), and its output is a local frequency (i.e., a physical layer signal that has a frequency and is local to this node) that is optionally propagated to downstream nodes. The noise process, e_{syncE}, represents the synchronous Ethernet phase noise accumulation in the synchronous Ethernet HRM (see Appendix II).

The residence time counter is incremented by the nominal period of the output clock of the EEC block. For example, if the output clock rate is 125 MHz, then the residence time counter is incremented by 8 ns each rising edge of the synchronous Ethernet output clock. Upon reception and transmission of PTP event messages, the residence time counter is sampled. The difference between the actual transmission/reception time and the sampled value of the time counter is modelled as e_{ts} since the transmission/reception event can happen between two rising edges of this clock. The effect of e_{ts} on the timestamp for reception of a PTP event message is added at the input, and the effect of e_{ts} on the timestamp for transmission of a PTP event message is added at the output. Note that e_{ts} for ingress and egress ports can be uncorrelated and can be of different polarity.

The noise process, $e_{phy,}$ represents the effect of asymmetry and timestamp sampling uncertainty on the PHY. The PHY latency asymmetry may be present if timestamping is done at a point other than the reference plane (i.e., the interface between the PHY and the physical medium). Any latency between the point where timestamping actually is done and the reference plane may be compensated for within PTP. However, any uncompensated latencies that result in asymmetry will contribute to e_{phy}. The noise, $e_{phy,}$ is added to the timing information contained in the incoming PTP messages. Note that the random process, $e_{phy,}$ may have a static component and a time-varying component.

The residence time counter produces a residence time. The input to the residence time counter is the frequency output of the EEC and the ingress and egress time for the PTP event frame.

The residence time counter is sampled upon reception of PTP event messages on ports. The residence time counter will add the accumulation of the synchronous Ethernet phase noise, $e_{syncE,}$ during the residence time.

Errors due to intranode transmission, $e_{intranode}$, and link asymmetry, $e_{link\text{-}asymm}$, must also be included. The latter is shown added to the output of the TC.

Figure I.5 is an equivalent model suitable for analytical studies.

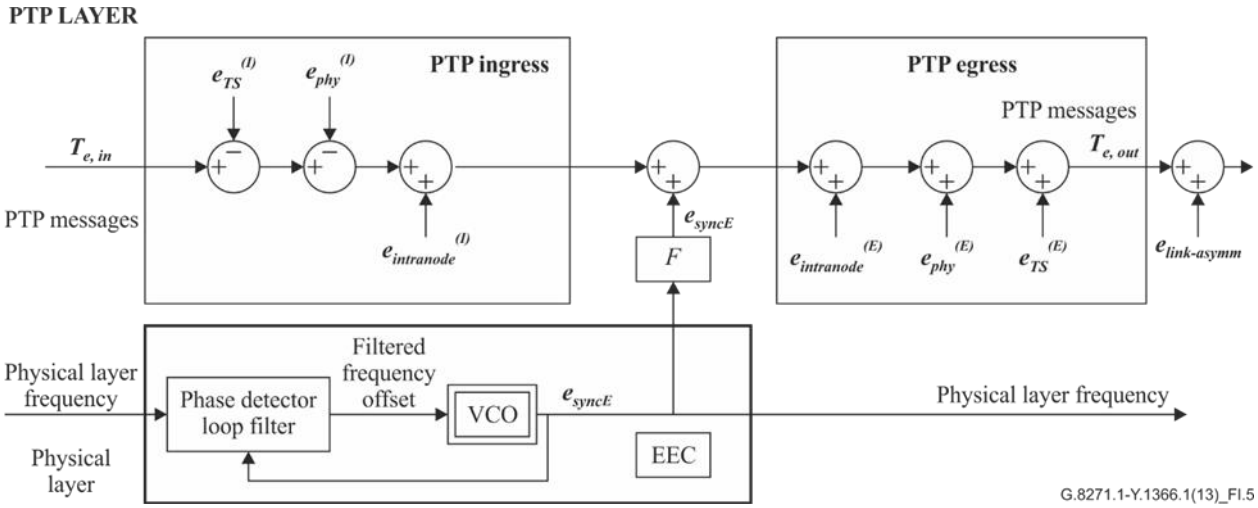


Figure I.5 – Telecom transparent clock model for analytical studies of the transport of time using PTP with synchronous Ethernet assistance.

In Figure I.5, the physical layer clock introduces a time error corresponding to the wander (e_{syncE}) that occurs between the ingress timestamp point and the egress timestamp point. This is equivalent to the time interval error over an observation interval equal to the packet's residence time. As a conservative approximation, this can be modelled as the change of the local clock's time error signal over the maximum allowed residence time *R*. In the figure above this is indicated by the operator *F*.

The value of the maximum residence time, *R*, is for further study. The model for a TC using a free running oscillator to measure the residence time can be modelled using the same model with the EEC replaced with a model for a free running oscillator. This is shown

in Figure I.6. For free-running oscillators that have a significant frequency offset, or for relatively large residence times, the error introduced may be dominated by this frequency offset.

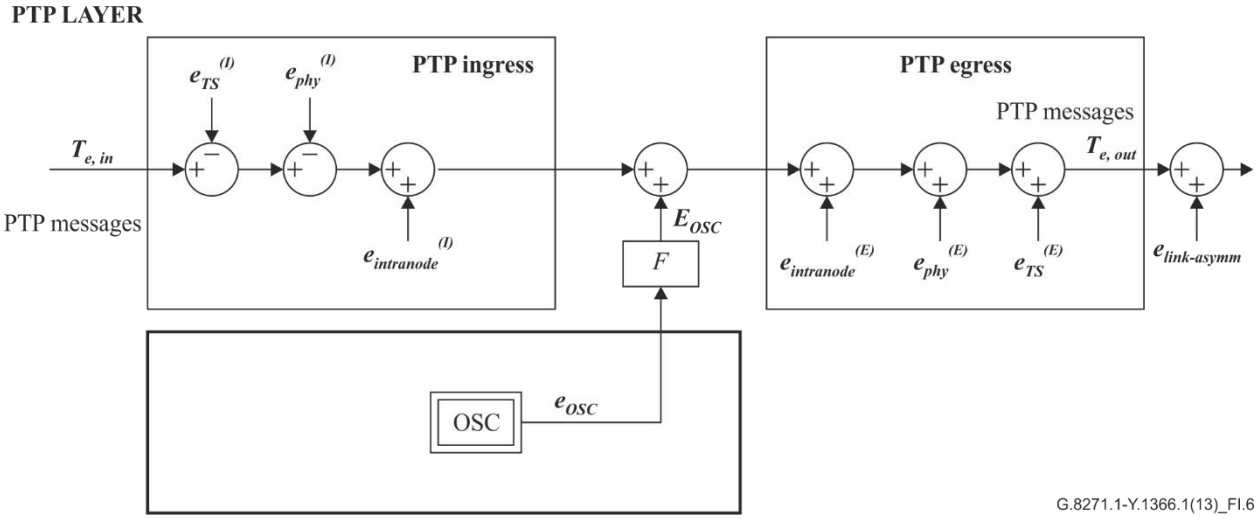


Figure I.6 – Telecom transparent clock model for analytical studies of the transport of time using PTP without synchronous Ethernet assistance

The simulation model for an end-to-end transparent clock using PTP for frequency reference (syntonized transparent clock) is for further study.

Appendix II

HRMs used to derive the network limits

(This appendix does not form an integral part of this Recommendation.)

II.1 HRM composed of T-BCs

The HRM models that are presented in the following caluses are applicable to the network reference models defined in Figure 4 of [ITU-T G.8271] and Figure 7-1 of this Recommendation. This is essential to derive the network limits between point 'B to C' when the packet network consists of network elements with T-BCs.

The purpose of these HRMs is to:

- establish reasonable worst-case network models for phase/time distribution using T-BCs;
- derive network limits and verify that they are consistent with performance requirements. Some of the performance requirements are summarized in Table 1 of [ITU-T G.8271];
- construct end-to-end phase and time error budget.

To determine the network limits, the most important aspects that need to be considered when a reference network is constructed are those that influence the accumulation of phase and time error of a reference "packet time signal" that is transported, and some of these are:

- specification of individual clocks and their noise specifications. In this case [ITU-T G.8273] shall be considered for the characteristics of the clock implemented in the T-BC. The model of the T-BC for noise accumulation simulations is described in Appendix I.
- the composition of a synchronization chain, cascade of clocks and ordering of clocks. This is defined by the related HRM.
- other sources of errors besides the noise generated by clocks. These are described in Appendix I of [ITU-T G.8271].

The following HRMs are based on a shorter chain of 12 clocks and a longer chain of 22 clocks.

II.1.1 HRM without physical layer frequency support from the network

The reference chain below shows a T-GM clock and a T-TSC interconnected by a number of T-BCs.

In this HRM-1 model, both frequency and time are transported via PTP. Both frequency and time follow the same synchronization path. The T-GM acts as both the source of frequency and time (e.g., the T-GM can receive its time and frequency from a global navigation satellite system (GNSS) receiver).

At the end of the chain, the phase/time reference is delivered to an end application (e.g., a mobile base station). Two cases are possible and are represented in the figure below:

1. The T-TSC is embedded in the end application.
2. The T-TSC is external to the end application, and delivers the phase/time reference to the end application via a phase/time synchronization distribution interface (e.g., 1 pulse per second (1 PPS) interface).

NOTE 1 – A specific equipment implementation may also be based on implementing a T-BC function (instead of a T-TSC function) and delivering the phase/time reference to the end application via a phase/time synchronization distribution interface.

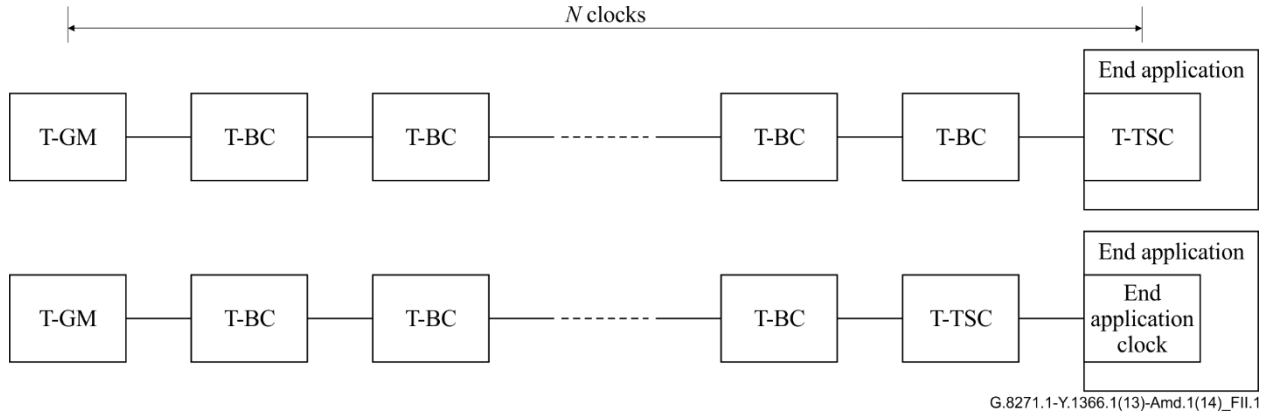


Figure II.1 – HRM-1 without physical layer frequency support

The number of clocks, *N*, cascaded in the HRM-1 for the shorter chain is 12. It corresponds to:

- one T-GM, ten T-BCs and one T-TSC for the case of a T-TSC embedded in the end application;

- one T-GM, nine T-BCs, one T-TSC and the end application clock for the case of a T-TSC external to the end application.

The number of clocks, *N*, cascaded in the HRM-1 for the longer chain is 22. It corresponds to:

- one T-GM, 20 T-BCs and one T-TSC for the case of a T-TSC embedded in the end application;
- one T-GM, 19 T-BCs, one T-TSC and the end application clock for the case of a T-TSC external to the end application.

NOTE 2 – Noise accumulation in networks without physical layer frequency synchronization support is for further study.

The physical layer connection between two T-BCs may not necessarily be Ethernet. For example, some T-BCs may be linked using microwave, xDSL, xPON or OTN technology. Such devices are called "media converters".

Figure II.2 shows a variation of the HRM where some unnamed technology is used to connect two of the T-BCs, or the T-BC and the T-TSC. The clock specification for the T-BC should be independent of the physical layer medium used for the connection.

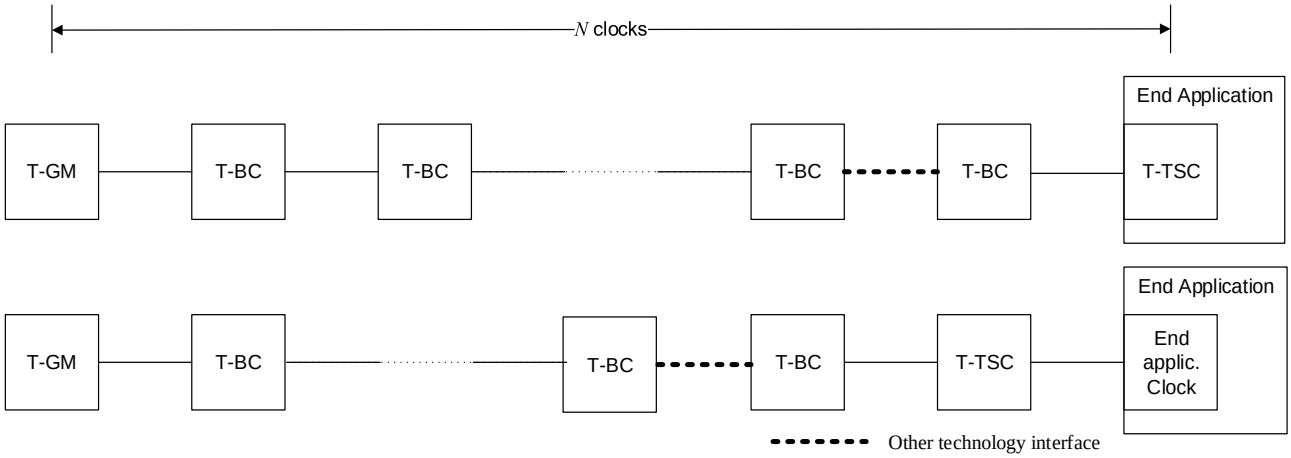


Figure II.2 – HRM-1, including some links using other technology interfaces

Where media converters are used in the network, the number N is for further study.

II.1.2 HRM with physical layer frequency support from the network

The reference chains below represent the cases where phase/time is transported via PTP and frequency via synchronous digital hierarchy (SDH)/synchronous Ethernet.

NOTE 1 – The analysis has been done with a synchronous Ethernet network based on option 1 EECs (see [ITU-T G.8262]).

Congruent scenario

In this HRM-2 model, both frequency and phase/time follow the same synchronization path.

At the end of the chain, the phase/time reference is delivered to an end application (e.g., a mobile base station). Two cases are possible and are represented in the figure below:

1. The T-TSC is embedded in the end application.
2. The T-TSC is external to the end application, and delivers the phase/time reference to the end application via a phase/time synchronization distribution interface (e.g., 1PPS interface).

NOTE 2 – A specific equipment implementation may also be based on implementing a T-BC function (instead of a T-TSC function) and delivering the phase/time reference to the end application via a phase/time synchronization distribution interface.

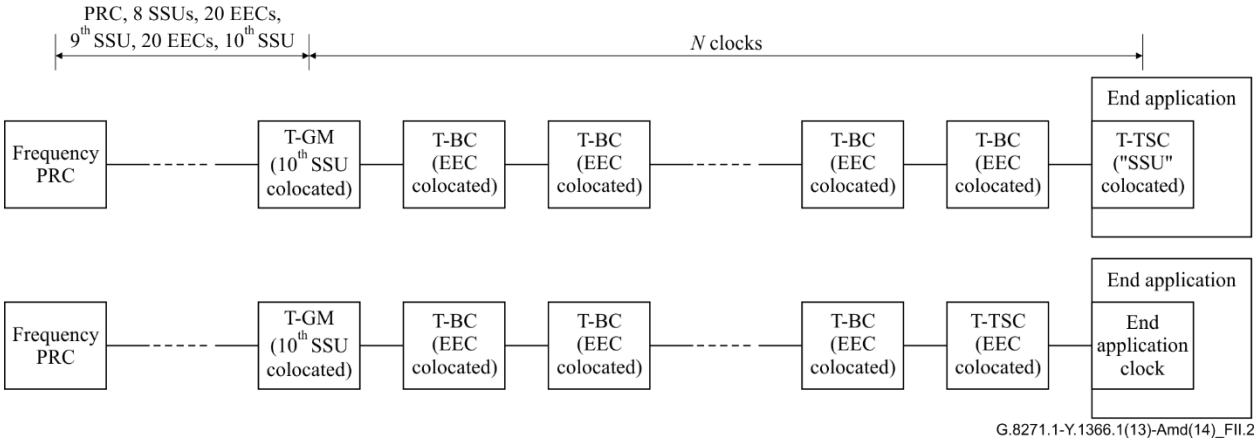


Figure II.3 – HRM-2 with physical layer frequency support – congruent scenario

The number of clocks, *N*, cascaded in the HRM-2 for the shorter chain is 12. It corresponds to:

- one T-GM, ten T-BCs and one T-TSC for the case of a T-TSC embedded in the end application;
- one T-GM, nine T-BCs, one T-TSC and the end application clock for the case of a T-TSC external to the end application.

The number of clocks, *N*, cascaded in the HRM-1 for the longer chain is 22. It corresponds to:

- one T-GM, 20 T-BCs and one T-TSC for the case of a T-TSC embedded in the end application;
- one T-GM, 19 T-BCs, one T-TSC and the end application clock for the case of a T-TSC external to the end application.

The following physical layer frequency clocks are co-located with the PTP clocks:

- for the T-GM: a synchronization supply unit (SSU) supporting phase/time transport;
- for the T-BC: an EEC supporting phase/time transport;
- for the T-TSC external to the end application: an EEC supporting phase/time transport;
- for the T-TSC embedded in the end application: the clock supporting phase/time transport is for further study. The initial assumption is that this clock might be close to the characteristics of an SSU (e.g., equivalent type of oscillator, but some characteristics of the clock may be different, e.g., different bandwidth). For the purpose of the simulations it is assumed that this clock is the only timing function of the end application (no other clock is cascaded after).

The SDH/synchronous Ethernet reference chain is a full [ITU-T G.803] reference chain with the EECs as close to the end of the chain as possible: a PRC, followed by 8 SSUs, followed by 20 EECs, followed by an SSU, followed by 20 EECs, followed by an SSU (co-located with the T-GM), followed by 9 EECs (each co-located with a T-BC) related to the shorter chain or 19 EECs (each co-located with a T-BC) related to the longer chain, followed by a final EEC (co-located with the T-TSC external to the end application or with a last T-BC). A final clock is at the end of the chain: either the "end application clock", or a clock co-located with the T-TSC embedded in the end application.

Non-congruent scenario

In this HRM-3 model, phase/time and frequency synchronization follow different synchronization paths (i.e., phase/time is distributed horizontally and frequency vertically). This model is similar in spirit to Figure A.1 of [ITU-T G.823] and is used to represent a possible worst-case scenario when PTP and SDH/synchronous Ethernet are used.

At the end of the chain, the phase/time reference is delivered to an end application (e.g., a mobile base station). Two cases are possible and are represented in the figures below:

1. The T-TSC is embedded in the end application;
2. The T-TSC is external to the end application, and delivers the phase/time reference to the end application via a phase/time synchronization distribution interface (e.g., 1PPS interface).

NOTE 3 – A specific equipment implementation may also be based on implementing a T-BC function (instead of a T-TSC function) and delivering the phase/time reference to the end application via a phase/time synchronization distribution interface.

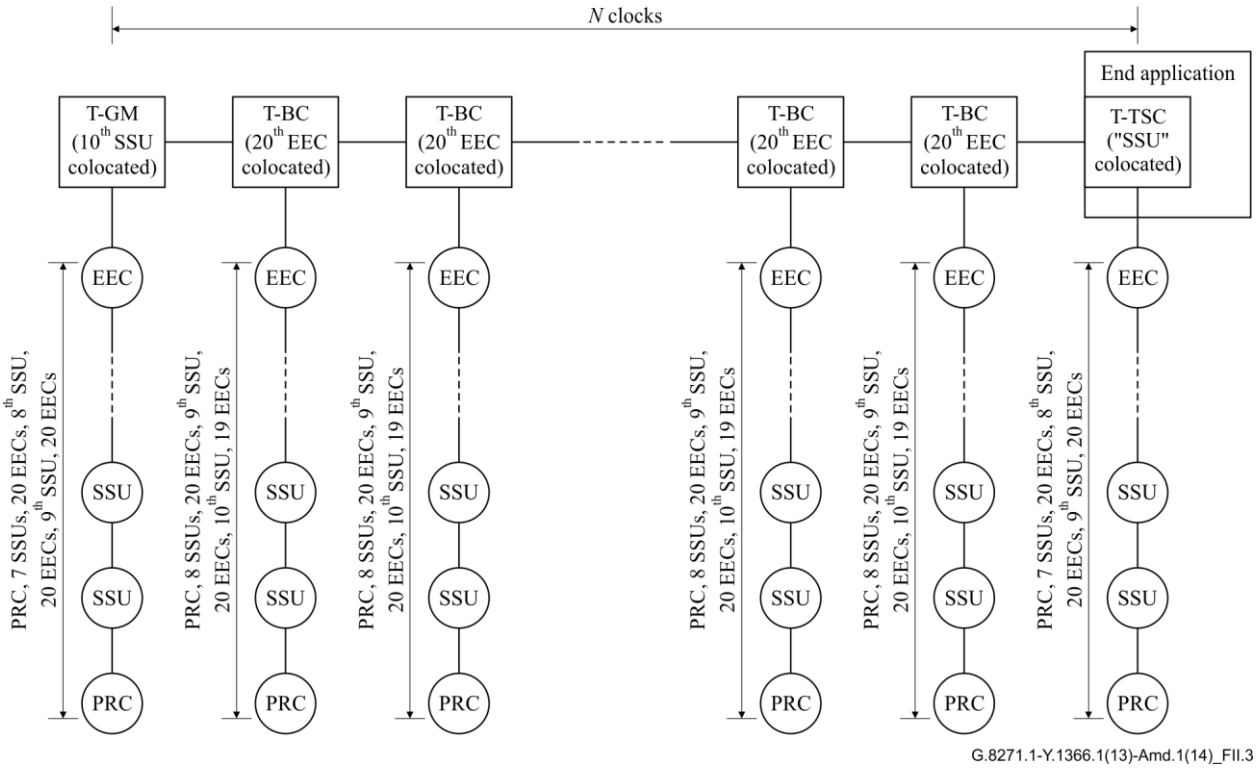


Figure II.4 – HRM-3 with physical layer frequency support –

non-congruent scenario, deployment case 1

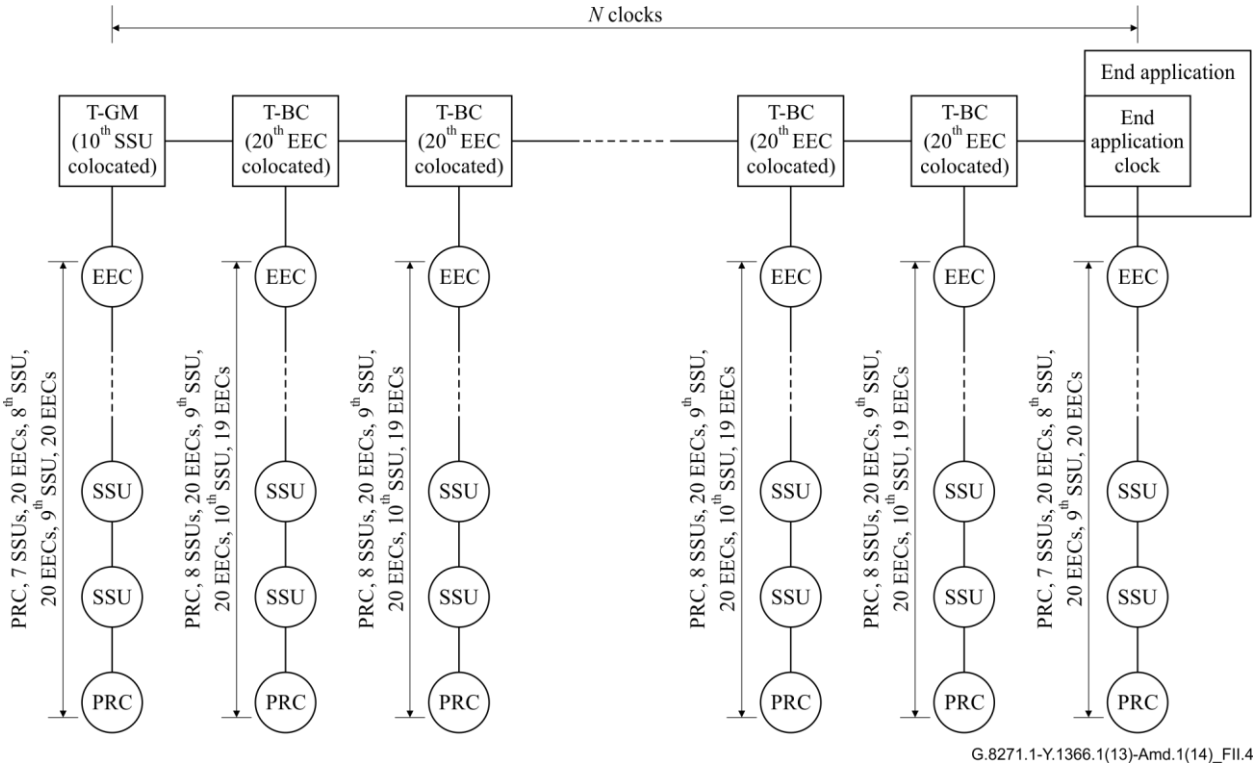


Figure II.5 – HRM-3 with physical layer frequency support –

non-congruent scenario, deployment case 2

The number of clocks, *N*, cascaded in the HRM-3 for the shorter chain is 12. It corresponds to:

- one T-GM, ten T-BCs and one T-TSC for the case of a T-TSC embedded in the end application;
- one T-GM, nine T-BCs, one T-TSC and the end application clock for the case of a T-TSC external to the end application.

The number of clocks, *N*, cascaded in the HRM-1 for the longer chain is 22. It corresponds to:

- one T-GM, 20 T-BCs and one T-TSC for the case of a T-TSC embedded in the end application;
- one T-GM, 19 T-BCs, one T-TSC and the end application clock for the case of a T-TSC external to the end application.

The following physical layer frequency clocks are co-located with the PTP clocks:

- for the T-GM: an SSU supporting phase/time transport;
- for the T-BC: an EEC supporting phase/time transport;
- for the T-TSC external to the end application: an EEC supporting phase/time transport;
- for the T-TSC embedded in the end application: the clock supporting phase/time transport is for further study. The initial assumption is that this clock might be close to the characteristics of an SSU (e.g., equivalent type of oscillator, but some characteristics of the clock may be different, e.g., different bandwidth). For the purpose of the simulations it is assumed that this clock is the only timing function of the end application (no other clock is cascaded after).

The SDH/synchronous Ethernet reference chain is a full [ITU-T G.803] reference chain with the EECs as close to the end of the chain as possible (the final SSU may be at the end of the chain):

- for the PTP clocks supported by an EEC: a PRC, followed by 8 SSUs, followed by 20 EECs, followed by an SSU, followed by 20 EECs, followed by an SSU, followed by 19 EECs with the 20th EEC being integrated in the T-BC or T-TSC clock;
- for the PTP clocks supported by an SSU: a PRC, followed by 7 SSUs, followed by 20 EECs, followed by an SSU, followed by 20 EECs, followed by an SSU, followed by 20 EECs with the 10th SSU being integrated in the T-GM or T-TSC clock .

II.1.3 HRM for cluster-based synchronization

The reference chain below shows a T-GM clock and a T-TSC interconnected by a number of T BCs. The reference chains are based on a longer chain of N clocks between the T-GM and T-TSC representing the joint part of the synchronization supply chain, which is common for all base stations and a shorter chain of M clocks between the part of the synchronization supply chain that is used for the specific base station only (which is part of the base station cooperation cluster). The number of clocks N cascaded in the longer chain and the number of clocks M cascaded in the shorter chain are independent to each other.

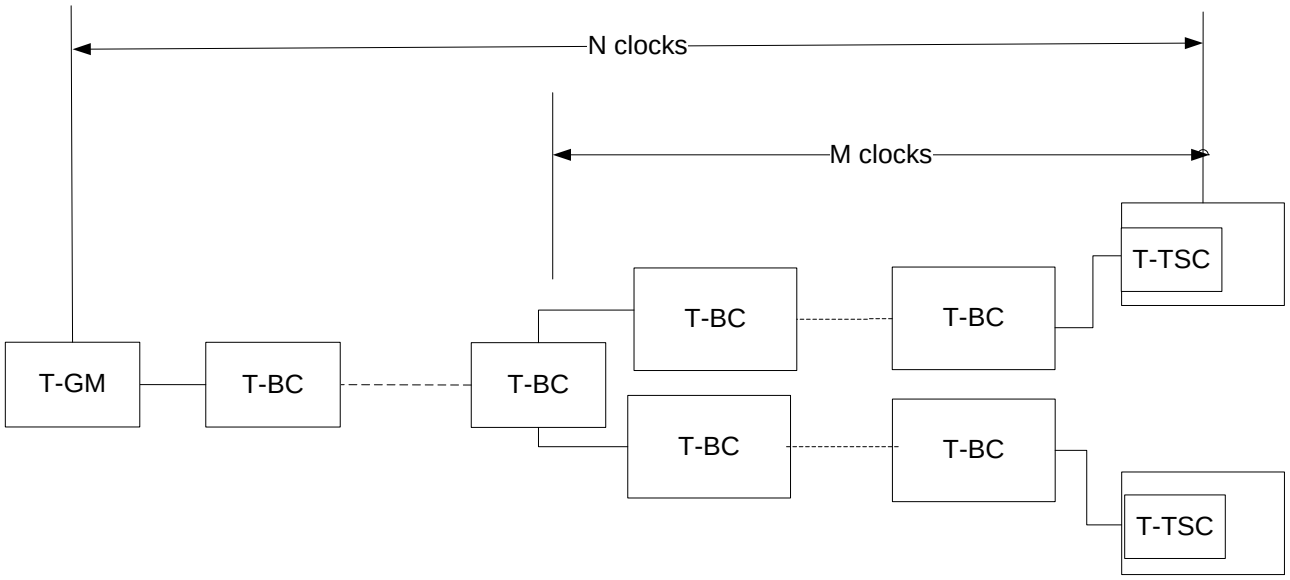


Figure II.6 – HRM-4 for cluster based synchronisation without physical layer frequency support

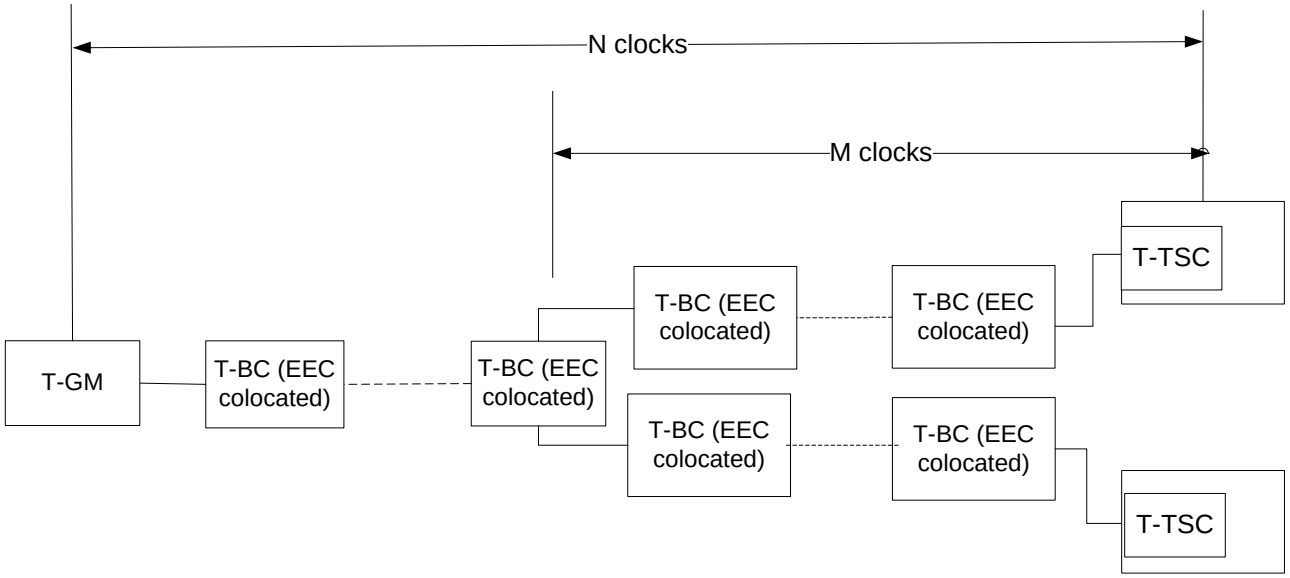


Figure II.7 – HRM-4 for cluster based synchronisation with physical layer frequency support

The number of clocks, N and M, are for further study.

The number of clocks, M, cascaded in the shorter chain in the HRM depends upon the specific application as per Table 2 of G.8271.

II.2 HRM composed of T-BCs and T-TCs

II.2.1 HRM with physical layer frequency support from the network

For the case of HRM with physical layer frequency support from the network, the same models as described in Figure II.3 and Figure II.4 apply where a maximum number of 8 T-TCs are included in the reference chain. Note: it is typical that the T-TCs are deployed close to the End Application. The T-TCs may be followed by T-BCs.

Appendix III

Network limits considerations

(This appendix does not form an integral part of this Recommendation.)

III.1 Measurement of network limits in case of deployment case 1

In the case of a network with full timing support and a T-BC as the last equipment of the chain, the measurement of the network limits for deployment case 1 at reference point C can be performed according to the following main approaches (note, telecom transparent clock (T-TC) may be integrated in the chain; this is for further study):

a) If available, via the output PPS test interface from the last BC of the chain (see Figure III.1). Note that, any additional source of error between the 1PPS measurement point and the actual reference point C has to be taken into account (e.g., link asymmetry).

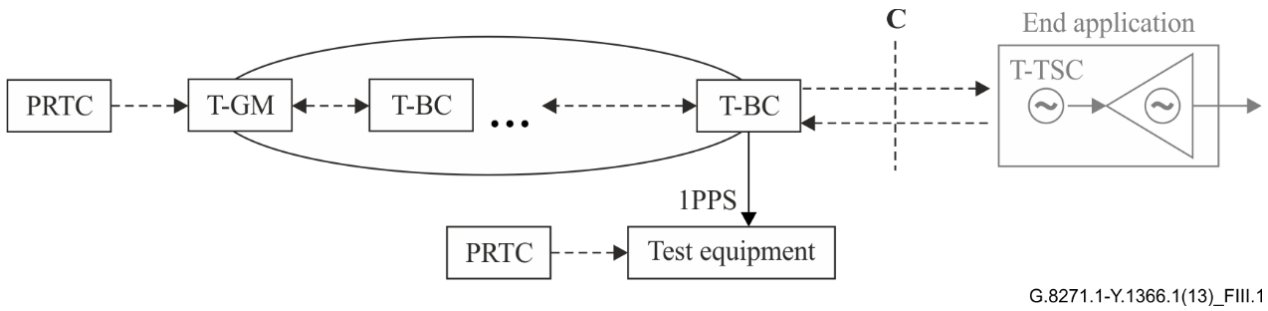


Figure III.1 – Deployment case 1 network limits measurement, option a)

b) Directly from the two-way PTP flow via a passive PTP monitor equipment (see "packet timing monitor" definition in [ITU-T G.8260]) connected to the test equipment. With the passive technique, a packet-based test device monitors packet exchanges over a communication link. In this way, the test device acts as an observer and it does not directly participate in the packet timing protocol, and there may be significant other non-synchronization-related traffic loading the T-BC port in addition to the synchronization packets of interest. This measurement can be performed by monitoring the outgoing Sync messages (and Follow_Up messages in case of two-steps clocks). Compensation for the additional delay between the T-BC output port and the test equipment is required. In particular, if the cable delay from the master port to the tap is known as "X" ns and the monitor establishes the time-of-passage of the Sync message at the tap as TM2 and extracts the time-of-departure from the master port as the time-stamp T1 (it may need to use the Follow_up), the forward time error of the master port is estimated as:

$$T_{fwd\_error} \approx (TM2 - T1 - X)$$

As an alternative, the packets in the reverse direction could also be used. In this case, the Delay Request messages can be timestamped by the PTP monitor with corresponding Delay Response messages providing timestamps from the T-BC. As before, compensation for the additional delay between the T-BC output port and the test equipment is required. For a cable delay of "X" ns, if the PTP Monitor timestamp of the Delay Request message is TM3 and the timestamp from the Delay Response message is T4, the reverse time error of the master port is estimated as the reverse time-stamp error:

$$T_{rev\_error} \approx (TM3 - T4 + X)$$

According to a further alternative approach the measurement can be performed using the full set of PTP messages exchanged between the T-TSC and the T-BC. In particular, the monitor establishes the time-of-passage of the Sync message at the tap as TM2 and reads the time-of-departure of the Sync message from the master port as T1. It also establishes the time-of-passage of the Delay_Request message at the tap as TM3 and reads the time-of-arrival of the Delay_Request message at the master port from the Delay_Response message as T4. Assuming that the packet rates in the two directions are the same and that the Sync message and Delay_Request message are close together in time, combined fwd/reverse time error, or time-transfer error, at the (master) port of the T-BC can be estimated as:

$$T_{combined\_error} \approx (TM2 - T1 - T4 + TM3)/2$$

The case where the forward and reverse packet rates are different, or require interpolation, is for further study.

The effective time error of the T-BC, $T_{err}(t)$ (either the forward time-stamp error, reverse time-stamp error or combined error) may be used to estimate the relevant metrics, such as the constant time error as described in [ITU-T G.8260].

It is noted that because this Recommendation addresses network performance requirements, it is expected that the three aforementioned error formulae provide equally valid estimates of the time error of the T-BC's internal clock.

Additional information regarding measurement of master port time-stamp error and time-transfer error is available in Annex A of [ITU-T G.8273].

This approach is described in Figure III.2.

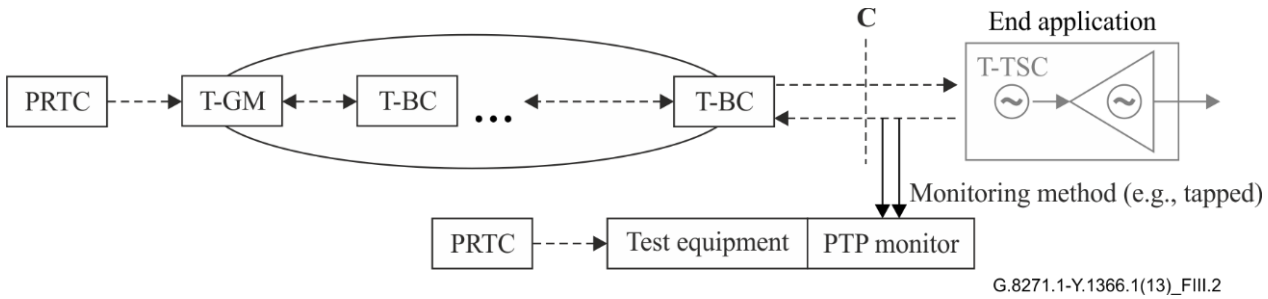


Figure III.2 – Deployment case 1 network limits measurement, option b)

c) From the two-way PTP flow via an active measurement probe (e.g., prior to the start of the service, or connecting the active monitor to a dedicated port of the T-BC). The measurement is performed using the full set of the PTP messages exchanged between the test equipment and the T-BC.

In particular, the monitor establishes the time-of- arrival of the Sync message as T2 and reads the time-of-departure of the Sync message from the master port as T1. It also establishes the time-of- departure of the Delay_Request message from the PTP Monitor as T3 and reads the time-of-arrival of the Delay_Request message at the master port from the Delay_Response message as T4. Assuming that the Sync message and Delay_Request message packet rates are the same and that the Sync message and Delay_request message are close together in time, an estimate of the time error at the port of the T-BC can be computed as:

$$T_{combined\_error} \approx (T2 - T1 - T4 + T3)/2$$

The case where the forward and reverse packet rates are different, or require interpolation, is for further study.

Additional information regarding measurement of the master port time-stamp error and time-transfer error is provided in [ITU-T G.8273] Annex A.

Assuming all ports of the T-BC behave similarly, the effective time error of the T-BC, $T_{err}(t)$ (either the forward time-stamp error, reverse time-stamp error or combined error) may be used to estimate the relevant metrics, such as the constant time error as described in [ITU-T G.8260].

This approach is described in Figure III.3.

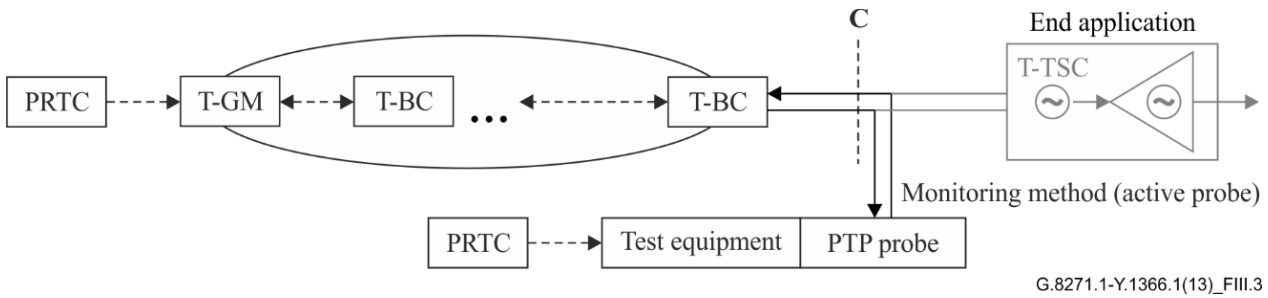


Figure III.3 – Deployment case 1 network limits measurement, option c)

In all cases the measurement is performed with respect to a PRTC.

Appendix IV

Constant and dynamic time error and error accumulation

(This appendix does not form an integral part of this Recommendation.)

IV.1 Introduction

Network limits for time error are expressed in terms of maximum absolute time error. That is, if time error measurement data is the sequence, $\{x(n\tau_0)\}$, the maximum absolute time error is

$$\max|TE| = \max_n |x(n\tau_0)| \quad \text{(IV-1)}$$

It may be advantageous to consider the time error in terms of "time-wander" and "time-jitter", representing the lower and higher frequency components of the time error. Denoting by $\{y(n\tau_0)\}$ the low-pass-filtered version of $\{x(n\tau_0)\}$, the maximum absolute time-wander is given by

$$\max|TE_W| = \max_n |y(n\tau_0)| \quad \text{(IV-2)}$$

where the subscript indicates that the measurement is related to time-wander. The Fourier frequency separating time-wander (the cut-off frequency of the low-pass filter) is for further study.

The time error measurement data, $\{x(n\tau_0)\}$, is generated either from the packet-based timing signal (e.g., PTP) or from a dedicated time output signal (e.g., 1PPS).

IV.2 Components of time error

The accumulated time error, $TE(t)$, at any reference point may be expressed in terms of a constant and a dynamic time error component, indicated as cTE and $dTE(t)$, respectively.

$$TE(t) = cTE + dTE(t) \quad \text{(IV-3)}$$

Constant time error, defined in [ITU-T G.8260], is a useful construct to express time error components that are immune to filtering. Such time error components are the result of, for example, asymmetry in the transmission medium between network elements, asymmetries within network elements, the beating effect in near-synchronous time-stamping, and so on. The power-spectrum of the constant time error is assumed to be equivalent to a delta function at $f = 0$ in the Fourier frequency domain.

The dynamic time error component, $dTE(t)$, is related to random noise accumulation (e.g., due to T-BC time-stamping or wander accumulated in the synchronous Ethernet network and injected into the time synchronization plane when synchronous Ethernet is used in combination with PTP or due to packet-delay variation experienced by the timing signal packets). The power spectrum of the dynamic time error is spread out over the Fourier frequency domain and the power can be reduced, to some extent, by low-pass filtering (e.g., as a result of the bandwidth of a given clock function within a network element).

To facilitate the analysis, it helps to further decompose the dynamic time error signal into two uncorrelated sub-components: $d^HTE(t)$ and $d^LTE(t)$ which represent the high and low frequency sub-bands of the dynamic time error, and where the bands are divided based on the bandwidth of the filter action of network element "i". Such decomposition is useful for analysing the accumulation of noise in a chain of time clocks. (Analysis of transient and hold-over budgets is also important, but is separate from this discussion). To a first approximation, the low-pass filter action of the network element can be modelled as an ideal low-pass filter with cut-off frequency B (Hz),

$$dTE(t) = d^LTE(t) + d^HTE(t) \quad \text{(IV-4)}$$

which separates the total time error into three components:

$$TE(t) = cTE + d^LTE(t) + d^HTE(t) \quad \text{(IV-5)}$$

The above decomposition of time error into three sub components is illustrated in the following table.

Table IV.1 – Decomposition of time error into sub-components

$TE(t)$	cTE	
	$dTE(t)$	$d^HTE(t)$
		$d^LTE(t)$

IV.3 Accumulation of time error in a chain of clocks

The accumulation of time error in a chain of clocks can be analysed in terms of the constant time error and dynamic time error components introduced above. It is important to note that the three components of time error described above accumulate differently. Specifically, the inherent low-pass nature of the clock filtering in a network element affects the incoming dynamic time error but passes

the incoming constant time error component essentially unchanged. Furthermore, the network element may add both constant and dynamic time error. One approach to illustrating the accumulation of time error is described with reference to Figure IV.1.

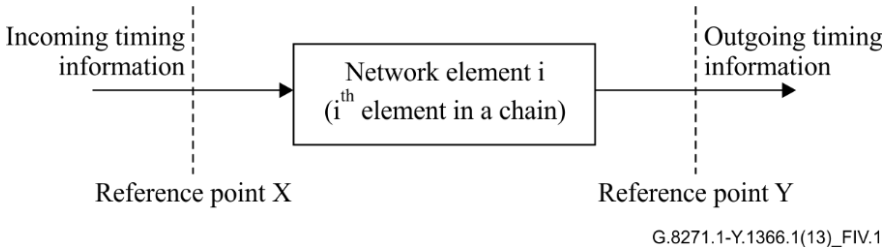


Figure IV.1 – Accumulation of time error

The maximum absolute time error at reference points X and Y are:

$$\max|TE_X(t)| = \max|cTE_X + dTE_X(t)| \quad \text{(IV-6)}$$

$$\max|TE_Y(t)| = \max|cTE_Y + dTE_Y(t)| \quad \text{(IV-7)}$$

where the subscripts "X" and "Y" indicates the value measured at reference points X and Y, respectively.

The constant time error at Y can be represented as the sum of the constant time error at X (cTE_X) plus the constant time error generated internally by the network element "*i*" (cTE_i)

$$cTE_Y = cTE_X + cTE_i \quad \text{(IV-8)}$$

The dynamic time error, dTE_Y, at Y is more complex, because a simple sum cannot be used. This is because the network element introduces a low-pass filter. As described above, the dynamic time error at X (the input of the network element "*i*") can be decomposed into high and low band sub-components:

$$dTE_X(t) = d^LTE_X(t) + d^HTE_X(t) \quad \text{(IV-9)}$$

and the dynamic time error introduced by the network element "*i*" can similarly be expressed in terms of low-frequency and high-frequency components as:

$$dTE_i(t) = d^LTE_i(t) + d^HTE_i(t) \quad \text{(IV-10)}$$

Then, the dynamic time error at Y (the output of the network element "*i*"), is a combination of the dynamic time error introduced by element "*i*" and the dynamic time error at X, the input dynamic time error being filtered by the processing of that element. The high band dynamic time error at X will, to a first approximation, be filtered out by the network element, while the low band dynamic time error at X will, to a first approximation, be passed through the network element. Low-band dynamic time error generated by the network element will, to some extent, be compensated by the time tracking action of the network element, but some residual low-band dynamic time error is expected to remain.

Therefore, we can represent the dynamic time error at Y in terms of the low band dynamic time error at X [$d^LTE_X(t)$], and the dynamic time error generated internally by network element "*i*" [$d^LTE_i(t)$ and $d^HTE_i(t)$]:

$$dTE_Y(t) \cong d^LTE_X(t) + d^LTE_i(t) + d^HTE_i(t) \quad \text{(IV-11)}$$

Substituting these two decompositions into the equation for maximum absolute time error at Y, we get the following expression:

$$max|TE_Y| = max|(cTE_X + cTE_i) + (d^LTE_X(t) + d^LTE_i(t)) + d^HTE_i(t)| \quad \text{(IV-12)}$$

Therefore, the maximum absolute time error at point Y depends on:

- the constant time error at X
- the constant time error introduced by network element "*i*"
- the low-band dynamic time error at X
- the dynamic time error introduced by network element "*i*" (low-band and high-band).

More generally, in a chain of time clocks, to a first order approximation:

- the constant time error, and link asymmetry, accumulates linearly
- the low-band dynamic time error accumulates incoherently
- the high-band dynamic time error is contributed mainly by the last element in the chain.

In a chain of time clocks, where the *N* nodes are indexed by the letter *i*, and the (*N*–1) links are indexed by the letter *j*, the maximum absolute time error at the output of the N^{th} node can be upper bounded as

$$\max\left|TE_N\right| \le \sum_{i=1}^{N}\left|cTE_i\right| + \sum_{j=1}^{N-1}\left|linkTE_j\right| + \sqrt{\left\{\sum_{i=1}^{N}\left[\max\left|d^LTE_i(t)\right|\right]^2\right\} + \left[\max\left|d^HTE_N(t)\right|\right]^2} \quad \text{(IV-13)}$$

here $linkTE_j$ denotes the asymmetry of link j, RSS denotes the square root of the sum of the squares of the N low-band dynamic time error contributions from each node, and the high-band dynamic time error of the last (N^{th}) node.

With this construct, constant time error accumulates coherently (simple summation) and dynamic time error accumulates incoherently (square-root of sum of squares) for the low band; the high band dynamic time error is present only as the contribution from the last stage. Stated differently, the mean values of the various sources of time error accumulate linearly and the variances of the various sources of time error accumulate linearly.

Therefore, the performance specification of a network element should include the following:

- maximum allowed constant time error generation;
- maximum allowed low and high band dynamic time error generation;
- dynamic time error bandwidth range (min/max);
- minimum dynamic time error input tolerance.

Appendix V

Example of design options

(This appendix does not form an integral part of this Recommendation.)

V.1 Network Limits

As described in Appendix IV, the network limits are expressed in terms of time error, and can be defined in one of three ways:

1. the maximum absolute time error, max |TE|
2. the dynamic time error component, $dTE(t)$;
3. the constant time error component cTE.

For example, the end application requirement, which for an LTE TDD network is 1.5µs, is an example of a maximum absolute time error limit. The MTIE mask in clause 7.3 of this Recommendation is an example of a dynamic time error limit.

V.2 Components of Time Error Budgets

A time error budget can be created for a network, working back from the end application requirement and subtracting out the time error generation introduced by various components. The components of the budget to be considered depend on the design of the operator's network. They may include the following elements:

- **Time error generation of the PRTC and T-GM**
  The max|TE| permitted for an integrated PRTC/T-GM combination is 100ns, as defined in [ITU-T G.8272]
- **Dynamic time error of the network of T-BCs, |dTE'|**
  The simulations performed have demonstrated that the maximum absolute dynamic time error, |dTE'| is less than 200ns for chains of up to 20 T-BCs.
  (Refer to Appendices I and II for further information on these simulations)
- **Constant time error of the T-BCs**
  The constant time error, cTE generated by a Type A T-BC is 50ns or less. cTE adds linearly with the number of T-BCs, therefore the cTE generated by a chain of 10 Type A T-BCs is up to 500ns.
  Similarly, the constant time error, cTE generated by a Type B T-BC, is 20ns or less; therefore, the cTE generated by a chain of 20 Type B T-BCs is up to 400ns.
  The cTE generated by a chain of clocks is denoted ce_{ptp_clocks}.
- **Constant time error of the links between network elements**
  The time offset estimation in PTP is unable to determine if the forward and reverse delays are asymmetric delays. Any difference in link delay between the forward and reverse directions will cause an error in a clock's calculation of time offset from master. This difference in delay may be caused by delays in the physical layer component, different wavelengths used in each direction, or differences in the lengths of the forward fibre compared to the reverse fibre.
  The cTE generated by the links in a chain denoted ce_{link_asyms}.
- **Transients caused by protection switching**
  There are several different failure scenarios that can be considered, and these are described in [ITU-T G.8275]. For example, physical layer assisted holdover may be used in the T-GM, to keep the internal clock "ticking" at a constant rate, or the PTP network may switch over to an alternative T-GM.
- **Noise generation of end application**
  Some allowance must be made for noise generation in the end application. In the case of an eNodeB, this is normally considered to be 150ns.

V.3 Failure Scenarios

There are three main failure scenarios considered here:

a. Failures in the synchronization network that cause the End Application clock to enter holdover for a short period. This is denoted TE_{REA} (rearrangement time error), which is provided by end application, and is normally considered to be less than 250ns.

   - As an example, this might be triggered by a loss of PRTC traceability of one of the redundant T-GMs in the network. The loss of traceability is indicated by the clockClass field carried in the Announce messages indicating a degraded quality level, and triggers the BMCA to run. If the clockClass is set to a value that is unacceptable to the End Application, then the clock will enter holdover for a short period (e.g. 1 minute) prior to synchronizing to another T-GM.

b. Failures in the synchronization network that do not cause the End Application clock to enter holdover. This is denoted TE_{HO} (holdover time error), which is provided by PRTC, and is normally considered to be less than 400ns.

- As an example, this might be related to a short interruption of the GNSS signal (e.g. 5 minutes), causing the PRTC to go into holdover for a short period. During this period, either a PRC-traceable synchronous Ethernet signal or a stable internal oscillator might be used as a back-up to the PRTC. In this case, the clockClass field continues to indicate an acceptable quality level so that the end application clock stays locked to the PTP reference.

c. Long interruption to the GNSS signal, with no alternative UTC-traceable T-GM available.
The long-term holdover condition is handled as a special case where the 1.5 µs limit is exceeded. This is assumed to be a particularly rare event.
The time error due to the holdover in this case, provided by PRTC, is assumed to be, in the worst case, 2'400 ns.

Further information on the protection scenarios and related budget is provided in this Appendix and in [ITU-T G.8275].

NOTE 1 – The end application is not required to handle long time synchronization holdover periods but only short interruptions that could be caused by network rearrangements. Time synchronization and rearrangements that may happen in the network and that are modeled by TE_{HO} are included in the network limits. As a first approximation, TE_{REA} and TE_{HO} shall not be considered at the same time; in fact, TE_{REA} assumes that the end application enters holdover as soon as a failure is detected in the network, while TE_{HO} assumes that the end application continues to be locked to the incoming reference and in this case there is no need to allocate a budget to TE_{REA}.

NOTE 2 – The time to restore (e.g., time to lock to a secondary time-synchronization reference) at the end application depends on the availability of physical frequency synchronization support and on the characteristics of the clock implemented in the end application.

V.4 Time Error Budget Allocation

The following table presents an example budget calculation related to the three failure scenarios.

Table V.1 – Example of time error allocation

Budget Component	**Failure scenario (a)** ***(T-GM rearrangement)***		**Failure scenario (b)** ***(Short GNSS interruption)***		**Failure scenario (c)** ***(Long holdover periods, e.g. 1 day)***	
PRTC (ce_{ref})	100 ns		100 ns		100 ns	
Holdover and Rearrangements in the network (TE_{HO})	NA		400 ns		2'400 ns	
Random and error due to synchronous Ethernet rearrangements (dTE')	200 ns		200 ns		200 ns	
Node Constant including intrasite (ce_{ptp_clock}) (Notes 1 and 2)	Type A 550 ns	Type B 420 ns	Type A 550 ns	Type B 420 ns	Type A 550 ns	Type B 420 ns
Link Asymmetries (ce_{link_asym}) (Note 3)	250 ns	380 ns	100 ns	230 ns	100 ns	230 ns
Network Limit at reference point C (TE_C)	**1100 ns**		**1350 ns (Note 4)**		**3350 ns**	
Rearrangements and short Holdover in the End Application (TE_{REA})	250 ns		NA		NA	
End application (TE_{EA})	150 ns		150 ns		150 ns	
Total Limit at reference point E (TE_E)	**1'500 ns**		**1'500 ns**		**3'500 ns (Note 5)**	

NOTE 1 – For Type A clocks, it is assumed in these examples that the clocks contribute constant TE of 50 ns as per type A T-BC (see [ITU-T G.8273.2]).

In deployment case 1 the HRM is composed of: 1 T-GM, 10 Type A T-BCs, 1 T-TSC (embedded in the end application) and 11 links.

In deployment case 2 the HRM is composed of: 1 T-GM, 9 Type A T-BCs, 1 T-TSC, 10 links and 1 intra-site link. The time error budget allocated to the time synchronization distribution in the intra-site connection between the packet clock and the end application in the worst case is 50 ns. Therefore the number of T-BCs is reduced by 1 to accommodate the extra time error resulting from the intra-site link.

Budget Component	Failure scenario (a) *(T-GM rearrangement)*	Failure scenario (b) *(Short GNSS interruption)*	Failure scenario (c) *(Long holdover periods, e.g. 1 day)*

NOTE 2 – For Type B clocks, it is assumed in these examples that the clocks contribute constant TE of 20 ns as per type B T-BC (see [ITU-T G.8273.2]).

In deployment case 1 the HRM is composed of: 1 T-GM, 20 T-BCs, 1 T-TSC and 21 links.

In deployment case 2 the HRM is composed of: 1 T-GM, 19 T-BCs, 1 T-TSC, 20 links and 1 intra-site link. The time error budget allocated to the time synchronization distribution in the intra-site connection between the packet clock and the end application in the worst case is 20 ns. Therefore the number of T-BCs is reduced by 1 to accommodate the extra time error resulting from the intra-site link.

NOTE 3 – The link asymmetry budget is the remainder after any asymmetry compensation has been included.

NOTE 4 – Failure scenario (b) may cause the network limit of 1'100 ns at point C to be exceeded. This is for further study.

NOTE 5 – Exceeding the TE_E limit of 1'500 ns may cause service degradation. The maximum frequency of occurrence of this scenario is governed by operator targets on service reliability.

V.5 Operator Options

The budget presented above is an informative example, demonstrating how an operator can construct a time error budget for the network.

Each operator can construct their own budget along similar lines. For example, if an operator used a smaller network with fewer nodes, then ce_{ptp_clock} (the sum of the constant time error from each clock) could be reduced. This either leaves a greater margin, or allows the link asymmetry budget (ce_{link_asym}) to be increased.

Operators may also choose different protection strategies. Some may prefer using PRC-traceable frequency assisted holdover in the T-GMs (i.e. scenario B), while others may choose to distribute more T-GMs around the network for immediate fail-over to an alternative T-GM (i.e. scenario A).

V.6 Further Details

As described in Appendix V.1, V.2, V.3 and V.5, the network limits are expressed in terms of the maximum time error, max |TE| and this is the result of two main components:

- the dynamic time error component, $dTE(t)$,
- the constant time error component cTE.

In order to take into account:

a. the internal noise sources of the end application, (indicated by TE_{EA}),

b. the residual noise caused by the dynamic time error component (indicated by dTE'),

c. short holdover at the End Application during rearrangements in the synchronization network (indicated by TE_{REA}), and

d. holdover in the synchronization network when the time reference is not available (indicated by TE_{HO}),

the network limit applicable at reference point C of deployment case 1 in figure 7-1, expressed in terms of maximum absolute time error, must satisfy the following relationships:

For case a):

$$\max |TE_C| + TE_{EA} + TE_{REA} \leq \max|TE_E|, \quad \text{(V-1a)}$$

with

$$|(cTE + dTE')| \leq \max |TE_C|. \quad \text{(V-2a)}$$

For case b):

$$\max |TE_C| + TE_{EA} \leq \max|TE_E|, \quad \text{(V-1b)}$$

with

$$|(cTE + dTE')| + TE_{HO} \leq \max |TE_C|. \quad \text{(V-2b)}$$

In the above, TE_E indicates the network limit at reference point E expressed in terms of maximum absolute time error, TE_{HO} represents the budget allocated to holdover and rearrangements in the network and $|dTE'|$ is the maximum absolute value of a

filtered version of the dynamic time error component $dTE(t)$. In practice *dTE'* estimates the dynamic component of the time error at the output of the End Application.

NOTE 1 - The network limit at reference point D of deployment case 2 in figure 7-2 is same with the above equations, except the terminology change of TE_C with TE_D.

NOTE 2 - the End Application is not required to handle long time synchronization holdover periods, but only short interruptions that could be caused by network rearrangements. Time synchronization and rearrangements that may happen in the network and that are modeled by TE_{HO} are included in the network limits. As a first approximation, TE_{REA} and TE_{HO} shall not be considered at the same time; in fact, TE_{REA} assumes that the End Application enters holdover as soon as a failure is detected in the network, while TE_{HO} assumes that the End Application continues to be locked to the incoming reference and, in this case, there is no need to allocate a budget to TE_{REA}.

NOTE 3 - the terms *cTE* and *dTE'* in the previous relationship are not measured separately, but indicate the components that build max |TE|. In the worst case, *cTE* and *dTE'* are both of the same polarity, but in a specific deployment they may partly compensate each other if the polarity is different.

The simulations performed have shown that is possible to limit $|dTE'|$ to 200 ns or less (i.e., in the worst case $|dTE'| = 200$ ns), and this value is considered in the time error budgeting analysis. Refer to Appendices I and II for further information on these simulations.

NOTE 4 – In order to meet the noise limit for the end application at reference point E, TE_E, the End application shall tolerate a certain amount of noise at its input (reference point C of deployment case 1 in figure 7-1, or reference point D of deployment case 2 in Figure 7-1). In case $dTE(t)$ exceeds the target limit of 200 ns, the end application should provide appropriate filtering to reduce the noise at reference point D to the value of *dTE'*, expressed in terms of maximum absolute time error. Further information is provided in Appendix VI.

NOTE 5 - the time to restore (e.g., time to lock to a secondary time-synchronization reference) at the end application depends on the availability of physical frequency synchronization support and on the characteristics of the clock implemented in the end application.

Based on (V-1a) and (V-2a), the following (V-3a) applies for case a),

$$|cTE| \leq TE_E - (TE_{EA} + TE_{REA} + dTE') \quad \text{(V-3a)}$$

And based on (V-1b) and (V-2b), the following (V-3b) applies for case b),

$$|cTE| \leq TE_E - (TE_{EA} + TE_{HO} + dTE') \quad \text{(V-3b)}$$

According to the assumption of $TE_E = 1500$ns, $TE_{EA} = 150$ns, $TE_{REA} = 250$ns, $TE_{HO} = 400$ns, and $dTE' = 200$ns, the following (V-4a) applies for case a),

$$|cTE| \leq 1500\text{ns} - (150\text{ns} + 250\text{ns} + 200\text{ns}) = 900\text{ns}, \quad \text{(V-4a)}$$

and the following (V-4b) applies for case b),

$$|cTE| \leq 1500\text{ns} - (150\text{ns} + 400\text{ns} + 200\text{ns}) = 750\text{ns} \quad \text{(V-4b)}$$

The constant time error component *cTE* is due to static contributions to the time error, mainly related to link asymmetries and PTP clock (T-BC, T-GM and T-TSC) constant time error accumulation.

NOTE 6 - *cTE* can be considered approximately constant over time assuming there are no changes in the network (e.g. re-routing).

In particular *cTE* can be expressed as follows:

$$|cTE| = ce_{ref} + ce_{ptp\_clocks} + ce_{link\_asyms}, \quad \text{(V-5)}$$

where ce_{ref} is the accuracy of the PRTC as specified in G.8272, ce_{ptp_clocks} is the sum of PTP clocks' constant time errors, which are defined as part of the T-BC specification, and ce_{link_asyms} is the overall time error due to link asymmetries. ce_{ptp_clocks} for m number of PTP clocks (T-GM, T-BC or T-TSC) in a chain can be expressed as follows:

$$ce_{ptp\_clocks} = \sum_{n=1}^{m} ce_{ptp\_clock,n}, \quad \text{(V-6)}$$

where $ce_{ptp\_clock,n}$ is the constant time error for the n^{th} PTP clock.

ce_{link_asyms} for m+1 number of links can be expressed as follows:

$$ce_{link\_asyms} = \sum_{n=1}^{m+1} ce_{link\_asym,n}, \quad \text{(V-7)}$$

where $ce_{link\_asym,n}$ is the time error due to link asymmetry for the n^{th} link.

Assuming Level of accuracy 4 as per Table 1/G.8271 (i.e. $TE_E = 1.5$ us) and $ce_{ref} = 100$ ns,the following applies for case a):

$$cTE = ce_{ref} + ce_{ptp\_clocks} + ce_{link\_asyms} \leq 900\text{ns} \quad \text{(V-8a)}$$

and therefore

$$ce_{ptp\_clocks} + ce_{link\_asyms} \leq 800 \text{ ns}, \quad \text{(V-9a)}$$

and the following applies for case b):

$$cTE = ce_{ref} + ce_{ptp\_clocks} + ce_{link\_asyms} \leq 750\text{ns}, \quad \text{(V-8b)}$$

and therefore,

$$ce_{ptp\_clocks} + ce_{link\_asyms} \leq 650 \text{ ns}. \quad \text{(V-9b)}$$

For the case of an HRM of 10 T-BCs, of constant TE of 50 ns (T-BC with Constant Time Error Class A, see [ITU-T G.8273.2]) and assuming that the constant time error for the T-GM also is 50 ns, this leads to

$$ce_{ptp\_clocks} = 50 \text{ ns} + (10 \times 50 \text{ ns}) = 550 \text{ ns} \quad \text{(V-10)}$$

And, for the case of an HRM of 20 T-BCs, of constant TE of 20ns (T-BC with Constant Time Error Class B, see [ITU-T G.8273.2]), and assuming that the constant time error for the T-GM also is 20ns, this leads to

$$ce_{ptp\_clocks} = 20 \text{ ns} + (20 \times 20 \text{ ns}) = 420 \text{ ns}. \quad \text{(V-11)}$$

Then the fiber asymmetry budget for case a), with T-BC Class A of [ITU-T G.8273.2], is

$$ce_{link\_asyms} \leq 250 \text{ ns}, \quad \text{(V-12a-1)}$$

and with T-BC Class B of [ITU-T G.8273.2] is

$$ce_{link\_asyms} \leq 380 \text{ ns}. \quad \text{(V-12a-2)}$$

The fiber asymmetry budget for case b) with T-BC Class A of [ITU-T G.8273.2] is

$$ce_{link\_asyms} \leq 100 \text{ ns}, \quad \text{(V-12b-1)}$$

and with T-BC Class B of [ITU-T G.8273.2] is

$$ce_{link\_asyms} \leq 230 \text{ ns}. \quad \text{(V-12b-2)}$$

Appendix VI

Mitigation of time error due to synchronous Ethernet transients

(This appendix does not form an integral part of this Recommendation.)

Appendix II, clause II.1.2 illustrates HRMs for the transport of phase/time via PTP with physical layer frequency support. Figure II.3 illustrates the congruent scenario, where the frequency and phase/time transports follow the same synchronization path. Figure II.4 illustrates the non-congruent scenario, where the frequency and phase/time transports follow different synchronization paths. A rearrangement of the physical layer frequency, e.g., synchronous Ethernet, transport results in phase/time error at each T-BC, the T-TSC, and the end application. The time error is generally larger in the congruent scenario than in the non-congruent scenario, because in the congruent scenario each T-BC has errors due to the rearrangement transient in both the time and frequency planes. The latter occurs in the physical layer frequency input to a T-BC, and the former occurs in PTP Sync messages input to a T-BC from the upstream T-BC. In the non-congruent scenario, a T-BC has an error due only to the physical layer frequency input (assuming that only one synchronous Ethernet reference chain at a time undergoes a rearrangement).

Details on requirements and solutions to address this issue are provided in [ITU-T G.8273.2].

NOTE 1 – In the case where in the congruent scenario the T-BC does not comply with [ITU-T G.8273.2] Annex B, the time error due to the synchronous Ethernet rearrangement can be reduced to an acceptable level by using an end application clock with sufficiently narrow bandwidth and sufficiently small gain peaking, and by collocating a suitable clock with the end application in the frequency plane. Simulations have shown that for the HRM of Appendix II, a maximum end application clock bandwidth of 0.005 Hz, with a maximum gain peaking of 0.1 dB, can reduce the time error due to the synchronous Ethernet rearrangement to an acceptable level. The analysis was done assuming an [ITU-T G.812] type I clock is collocated with the end application clock in the frequency plane; however, a different type of clock might still result in an acceptable time error. This has not been verified.

In the non-congruent scenario, the time error will be acceptable if the T-BCs, T-TSC, and end application have minimum bandwidth of 0.05 Hz, maximum bandwidth of 0.1 Hz and maximum gain peaking of 0.1 dB, and if the frequency plane clocks collocated with the T-BCs, T-TSC, and end application are EECs. This is true whether or not the synchronous Ethernet transient is rejected at each T-BC.

NOTE 2 – The case of a network where synchronization status message (SSM) is not used is for further study.

Appendix VII

Maximum relative time error

(This appendix does not form an integral part of this Recommendation.)

Time errors (accuracy) could also be expressed in terms of maximum relative time error, rather than maximum absolute time error, which is described in Appendix IV. However, in order to calculate the relative time error, it is necessary to calculate the absolute time error as well.

Now, in order to calculate the maximum relative time error accuracy, one approach to illustrating the accumulation of relative time error is described with reference to Figure VI.1.

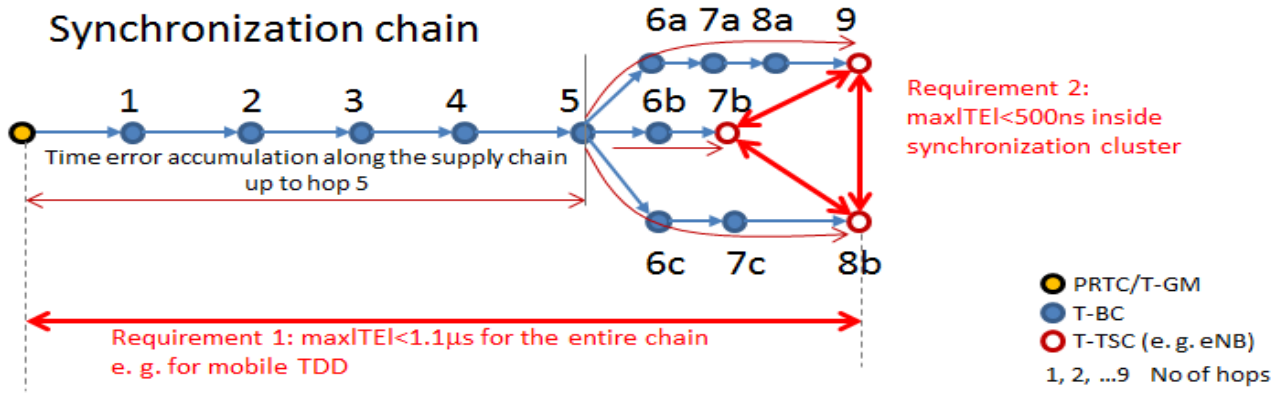


Figure VII.1 – Illustration of Relative Time Error

In figure VI.1, nodes 1 to 5 represent the joint part of the synchronization supply chain, which is common for all base stations. Nodes 5 to 6(a, b, c)/7(a, b, c)/8(a, b)/9 represent the part of the synchronization supply chain that is used for the specific base station only (which is part of the base station cooperation cluster). Time error components from the common used synchronization chain, such as cTE, do influence all base stations of the synchronization cluster in the same way. That is, from figure VI.1, the entire chain requires 1.1 µs as max|TE| for the entire chain due to TDD operation., In addition, a maximum relative Time Error of 500 ns maximum deviation between the end applications is required inside the synchronization cluster.

From figure VI.1, the maximum absolute time error at reference points 5/6(a, b, c)/7(a, b, c)/8(a, b)/9 is:

$$\max|TE_X(t)| = \max|cTE_X + dTE_X(t)| \quad \text{(VI-1)}$$

where X represents the reference points 5/6(a, b, c)/7(a, b, c)/8(a, b))/9 at which the maximum absolute time error is measured. Now, the maximum relative time error is related to the maximum deviation (time error) between adjacent base stations that are present in the same synchronization cluster, obtaining their frequency and phase synchronization from the same source for the last network elements in the chain.

Firstly, the relative time error between node X and node Y is,

$$TE_{xy}(t) = TE_x(t) - TE_y(t) \quad \text{(VI-2)}$$

And, the maximum absolute relative time error is,

$$\mathbf{\max|TE_{xy}(t)| = \max|TE_x(t) - TE_y(t)|} \quad \mathbf{(VI\text{-}3)}$$

In addition, the maximum time error can be also denoted by Eq. (VI-4) and Eq. (VI-5)

$$TE_x(t) = TE_z(t) + TE_{xz}(t) \quad \text{or} \quad TE_{xz}(t) = TE_x(t) - TE_z(t) \quad \text{(VI-4)}$$

$$TE_y(t) = TE_z(t) + TE_{yz}(t) \quad \text{or} \quad TE_{yz}(t) = TE_y(t) - TE_z(t), \quad \text{(VI-5)}$$

where:

$TE_z(t)$, $TE_x(t)$ and $TE_y(t)$ are the absolute time errors at node Z, node X and node Y, respectively. The node Z, e.g., node 5 in Figure VI.1, connects with both node X and node Y, and

$TE_{xz}(t)$ is the relative time error between node X and node Z,

$TE_{yz}(t)$ is the relative time error between node X and node Z.

Substituting Eq. (VI-4) and Eq. (VI-5) into Eq. (VI-2) gives

$$\begin{aligned} TExy(t) &= TEx(t) - TEy(t) \\ &= (TEz(t) + TExz(t)) - (TEz(t) + TEyz(t)) \\ &= TExz(t) - TEyz(t) \end{aligned} \quad \text{(VI-6)}$$

Then, the maximum absolute relative time error is

$$\max|TE_{xy}(t)| = \max|TE_x(t) - TE_y(t)|$$

$$= \max| TE_{xz}(t) - TE_{yz}(t) | \quad \text{(VI-7)}$$

A well-known property of inequalities involving real numbers is

$$|u - v| \le |u| + |v| \quad \text{(VI-8)}$$

for any real numbers *u* and *v*.

Then:

$$| TE_{xz}(t) - TE_{yz}(t) | \le | TE_{xz}(t) | + |TE_{yz}(t) | \quad \text{(VI-9)}$$

and:

$$\max| TExz(t) - TEyz(t) | \le \max(| TExz(t) | + |TEyz(t) |) \quad \text{(VI-10)}$$

In addition, for any two real-valued functions, $f(t)$ and $g(t)$:

$$\max(f(t) + g(t)) \le \max(f(t)) + \max(g(t)) \quad \text{(VI-11)}$$

Then, using Eq. (VI-11) in Eq. (VI-10) produces :

$$\max| TE_{xz}(t) - TE_{yz}(t) | \le \max| TE_{xz}(t) | + \max|TE_{yz}(t) |). \quad \text{(VI-12)}$$

Appendix VIII

Models for Budgeting in a chain of Microwave Devices

(This appendix does not form an integral part of this Recommendation.)

Figures VIII.1 and VIII.2 below show the topology to be considered when developing budgets for chains of microwave equipment functioning as chains of T-BCs.

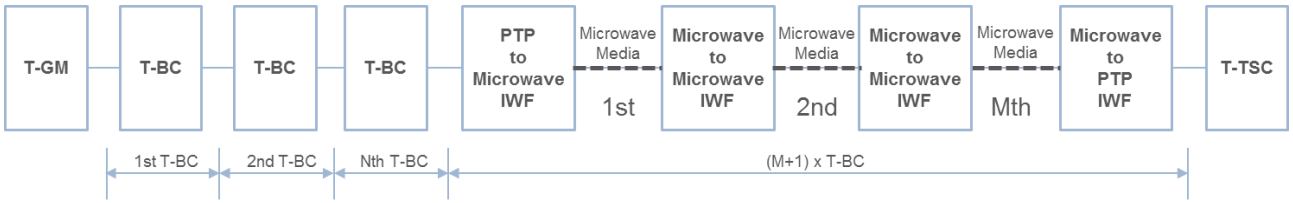


Figure VIII.1: Network reference model for phase/time synchronization over *M* microwave hops

The case of cascaded Microwave links where microwave links are alternated with Ethernet based equipment or in general where the microwave equipment are connected via Ethernet and PTP is carried over Ethernet, can be modelled by the following figure showing *N* cascaded T-BCs combined with *M* microwave links.

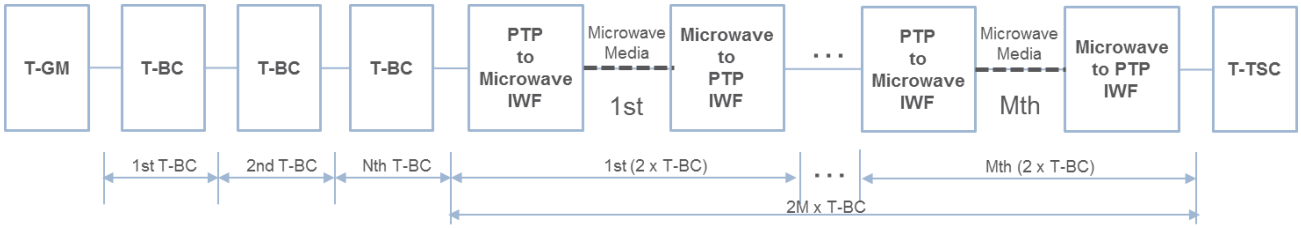


Figure VIII.2: Network reference model for phase/time synchronization over *M* microwave hops, including intermediate conversion between Microwave to Ethernet

NOTE 1: similar topology can be considered when developing budgets for chains of microwave equipment functioning as chains of T-TCs (i.e., replacing T-BC with T-TC in figures VIII.1 and VIII.2).

NOTE 2: This does not require that each microwave equipment (transmitter, repeater or receiver) must function as a PTP BC or TC. The equivalence to a T-BC or T-TC is purely for performance estimation purposes as part of the HRM.

Figure VIII.3 shows an example of equipment that is transferring timing flow from native PTP to native access media, such as microwave equipment. Only one PTP port and one Special port are shown in the diagram, although the equipment may contain multiple ports.

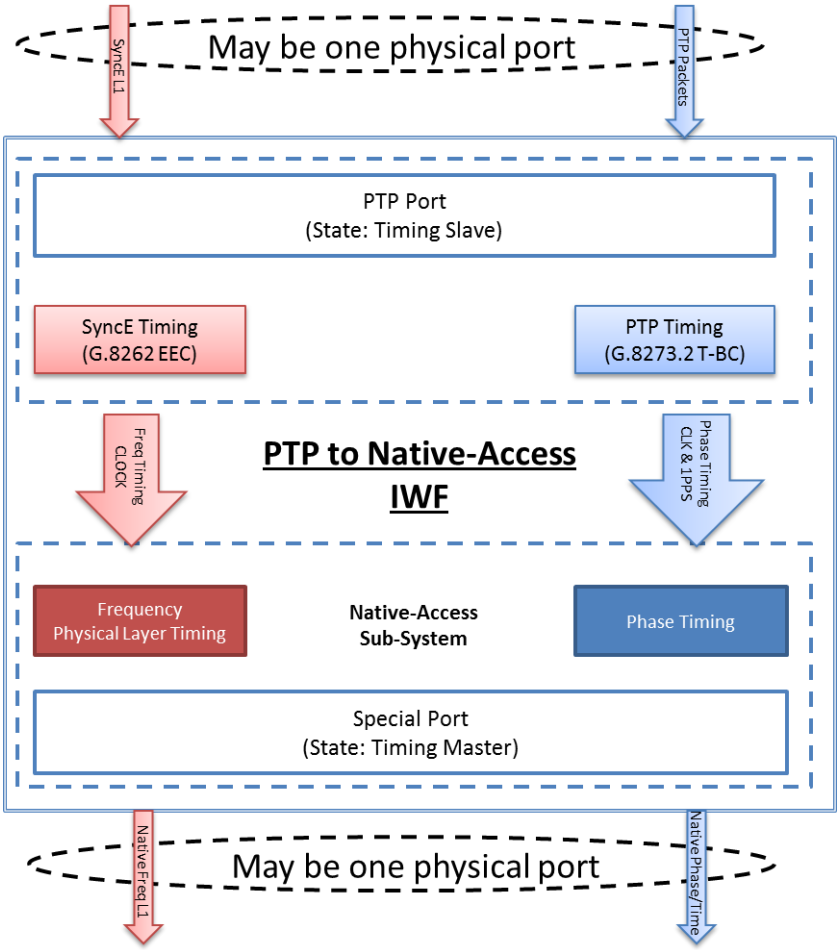


Figure VIII.2: Timing Flow from PTP to Native Access Media (Either Direction)

NOTE: In the above diagram an example is shown with one physical port on each side

Figure VIII.4 shows an example of equipment that is transferring timing flow from native access media to PTP, such as microwave equipment. Only one PTP port and one Special port are shown in the diagram, although the equipment may contain multiple ports.

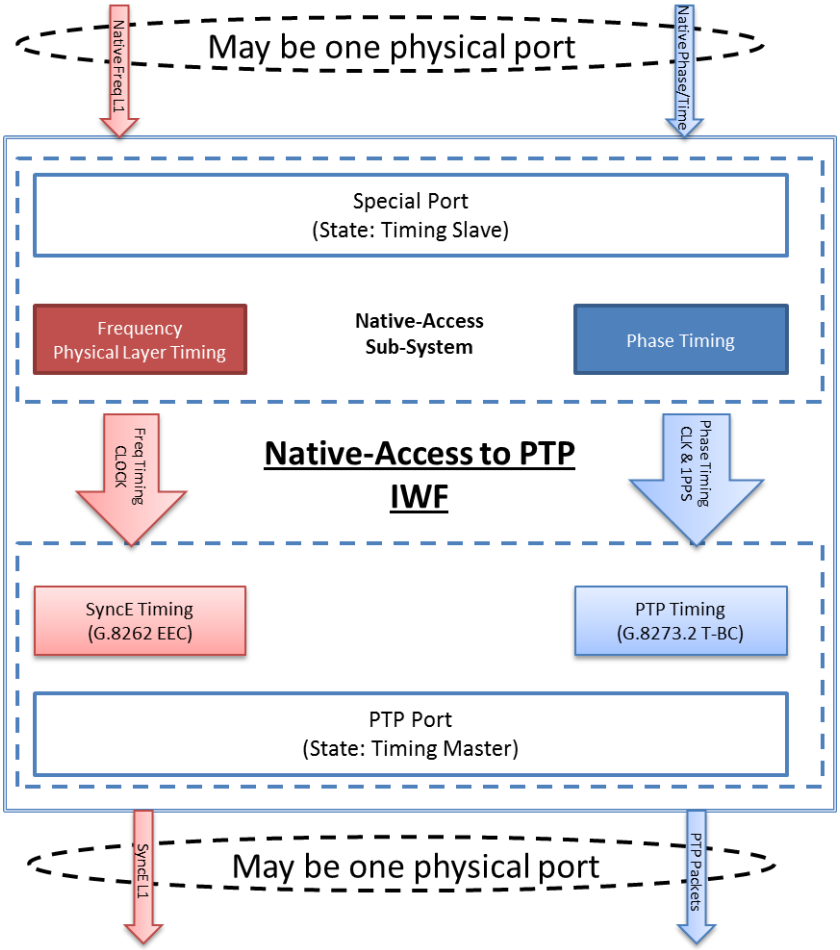


Figure VIII.3: Timing Flow from Native Access Media to PTP (Either Direction)

NOTE: In the above diagram an example is shown with one physical port on each side

Appendix IX

Models for Budgeting in a chain of xPON or xDSL Devices

(This appendix does not form an integral part of this Recommendation.)

Figure IX.1 below shows the topology to be considered when developing budgets for chains of native access equipment (such as xPON or xDSL) functioning as chains of T-BCs.

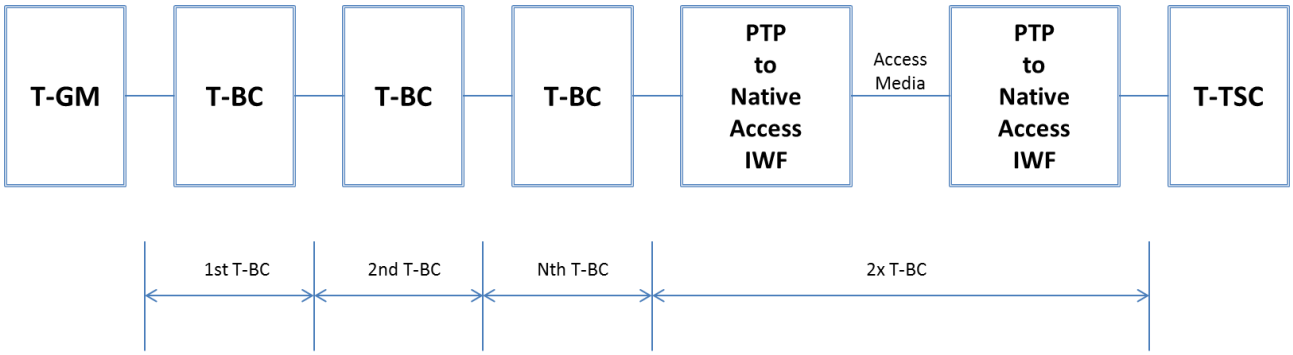


Figure IX.1: Network reference model for phase/time synchronization over native access media

As shown in Figure IX.1, the same performance budget of the equivalent of two T-BCs may be used when developing performance budgets for access systems, e.g. xPON or xDSL. This is purely for performance estimation purposes; it does not mean that each unit (e.g. OLT and ONT in a GPON system) has to actually function as a PTP BC.

When measuring the performance of a GPON system, it should be fully loaded with ONTs for worst-case noise generation.

Figure IX.2 shows an example of equipment that is transferring timing flow from native PTP to native access media, such as xPON OLT or xDSL DSLAM equipment. Only one PTP port and one Special port are shown in the diagram, although the equipment may contain multiple ports.

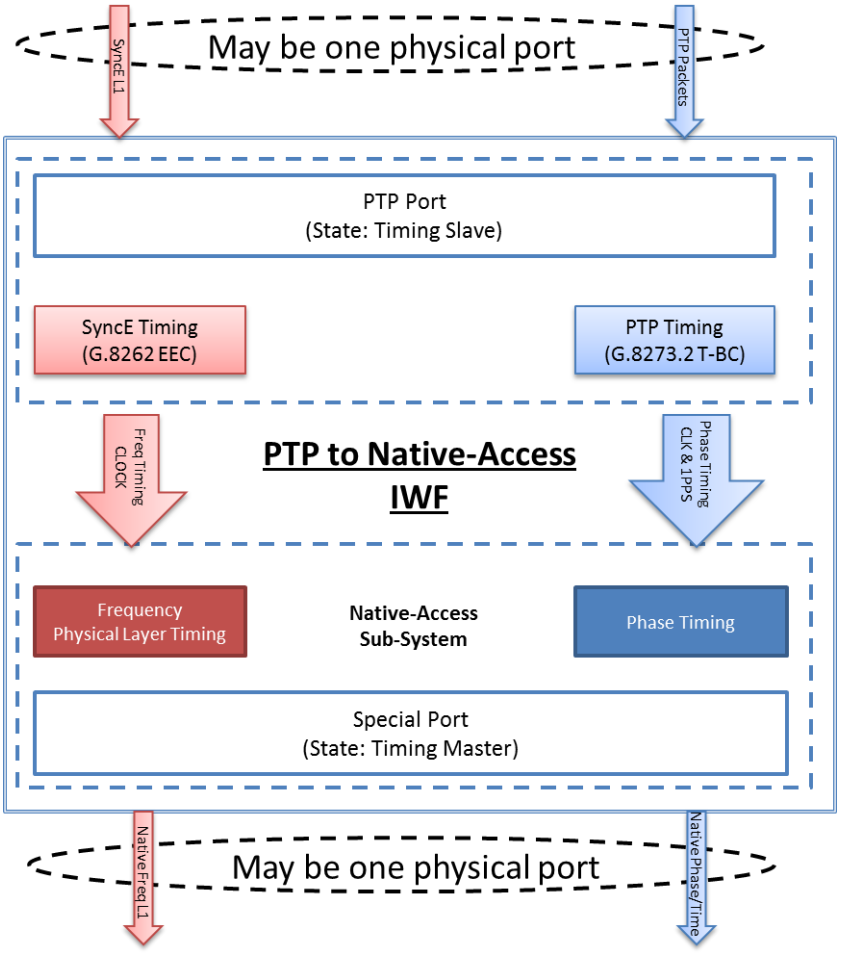


Figure IX.2: Timing Flow from PTP to Native Access Media (Downstream)

NOTE: In the above diagram an example is shown with one physical port on each side

Figure IX.3 shows an example of equipment that is transferring timing flow from native access media to PTP, such as xPON ONU or xDSL RT-DSLAM equipment. Only one PTP port and one Special port are shown in the diagram, although the equipment may contain multiple ports.

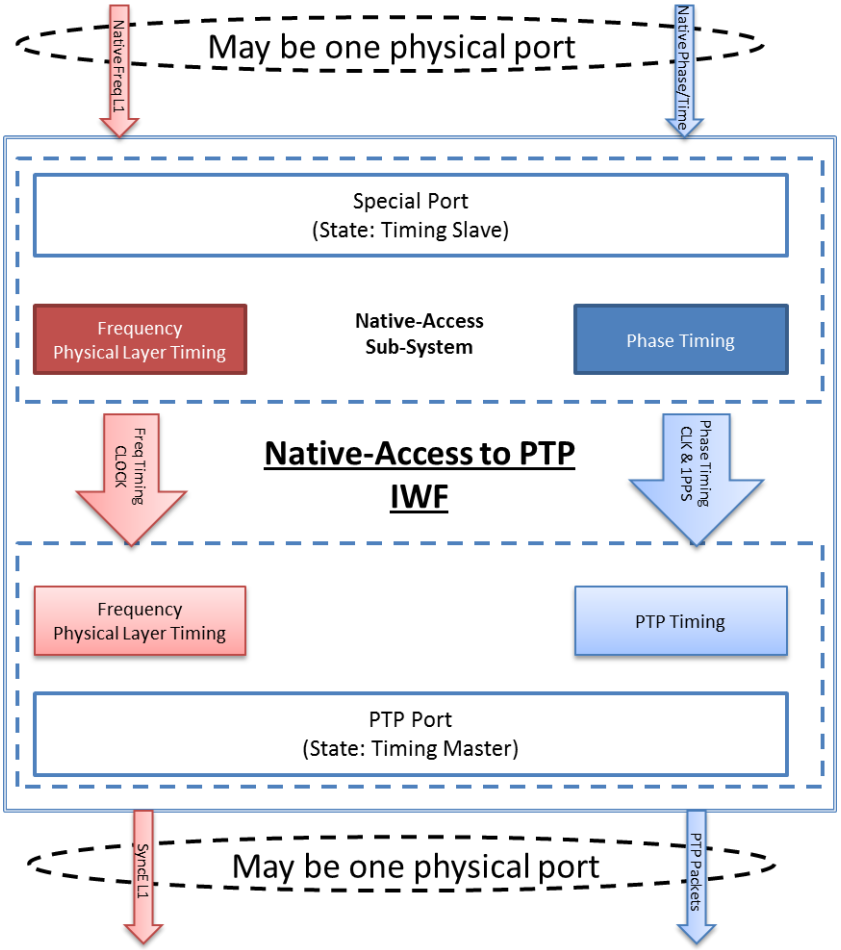


Figure IX.3: Timing Flow from Native Access Media to PTP (Downstream)

NOTE: In the above diagram an example is shown with one physical port on each side